**Tennessee Tech
UNIVERSITY**

Time-Reversal Based Range Extension Technique for Ultra-wideband (UWB) Sensors and Applications in Tactical Communications and Networking

Technical Report (Quarterly)

to

US Office of Naval Research

875 North Randolph Street

Arlington, VA 22203-1995

for

Grant # N00014-07-1-0529

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July 16, 2007

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20070924084

REPORT DOCUMENTATION PAGE

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.
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1. REPORT DATE (DD-MM-YYYY)	2. REPORT TYPE	3. DATES COVERED (From - To)
16-07-2007	Technical Report (Quarterly)	April 16, 2007--July 16, 2007

4. TITLE AND SUBTITLE	5a. CONTRACT NUMBER
Time-Reversal Based Range Extension Technique for Ultra-wideband (UWB) Sensors and Applications in Tactical Communications and Networking	
	5b. GRANT NUMBER N00014-07-1-0529
	5c. PROGRAM ELEMENT NUMBER
6. AUTHOR(S) Qiu, Robert C.; Guo, Nan; Zhang, Qiang; Zhou, Chenming; Hu, Zhen; Zhang, Peng; Singh, Dalwinder; Corey Cooke.	**5d. PROJECT NUMBER**
	5e. TASK NUMBER
	5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)	8. PERFORMING ORGANIZATION REPORT NUMBER
Tennessee Technological University 115 W. 10th Street Cookeville, TN 38501	

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)	10. SPONSOR/MONITOR'S ACRONYM(S)
US Office of Naval Research 875 North Randolph Street Arlington, VA 22203-1995	ONR
	11. SPONSOR/MONITOR'S REPORT NUMBER(S) 07PR05074-00

12. DISTRIBUTION/AVAILABILITY STATEMENT

release for public distribution.

13. SUPPLEMENTARY NOTES

14. ABSTRACT

This technical report (quarterly) details the work for Office of Naval Research (ONR) by Tennessee Tech. The goal of this project—jointly funded by ONR, NSF, and ARO—is to build a general purpose testbed with time reversal capability at the transmitter side. The envisioned application is for UWB sensors and tactical communications in RF harsh environments where multipath is rich and can be exploited through the use of time reversal. The report summarizes the results for each of three major tasks. The central task of this project is to address unique (rich) multipath problem faced with system design and implementation. The 1G testbed is working over the air and almost finished–except for an issue related to the high-speed interface between the FPGA and A/D converter. Currently, the 2G testbed is ongoing and very unstable—we are integrating the transmitter system in our Lab. More details are expected to be reported in the next report.

15. SUBJECT TERMS

UWB, testbed, time reversal, range extension, sensors

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			Francis Otuonye
U	U	U	UU	24	**19b. TELEPHONE NUMBER** (Include area code) 931-372-3374

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Acknowledgment

Executive Summary

This technical report (quarterly) details the work for Office of Naval Research (ONR) by Tennessee Tech. The goal of this project—jointly funded by ONR, NSF, and ARO—is to build a general purpose testbed with time reversal capability at the transmitter side. The envisioned application is for UWB sensors and tactical communications in RF harsh environments where multipath is rich and can be exploited through the use of time reversal. The report summarizes the results for each of three major tasks. Specifically, the project can be broken into

- Task 1–Time Reversal MIMO Performance (Chapter 2)
- Task 2–Design Consideration of Transceiver Technology for Second Generation (2G) Testbed (Chapter 3)
- Task 3– First Generation (1G) System Testbed (Chapter 4)

The central task of this project is to address unique (rich) multipath problem faced with system design and implementation. The 1G testbed is working over the air and almost finished–except for an issue related to the high-speed interface between the FPGA and A/D converter. Currently, the 2G testbed is ongoing and very unstable—we are integrating the transmitter system in our Lab. More details are expected to be reported in the next report.

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Contents

Chapter 1

Introduction

This technical report (quarterly) details the work for Office of Naval Research by Tennessee Tech [1]. This report—the second quarterly technical report for this UWB time reversal testbed project, started January 16 2007—summarizes the results for each of three major tasks. Specifically, the project can be broken into

- Task 1–Time Reversal MIMO Performance (Chapter 2)
- Task 2–Design Consideration of Transceiver Technology for Second Generation (2G) Testbed (Chapter 3)
- Task 3– First Generation (1G) System Testbed (Chapter 4)

The central task of this project is to address unique (rich) multipath problem faced with system design and implementation [3] [6]. UWB is a system with a bandwidth of more than 500 MHz. It is very challenging [2] [3] [5]. One point-to-point system is considered in this report. For multiple user time reversal, the audience is referred to [17].

Roughly speaking, the research in the report is driven by the following understanding. First, a UWB channel experiences unique propagation phenomenon—pulse shape distortion due to selective frequency attenuation and extremely rich multipath. Fundamental system limits benefit from multipath. The good news is that fading seems not be an major issue for a UWB system. Second, when a coherent receiver such as RAKE is used, the implementation complexity is too high. Third, people seek non-coherent transceiver solutions, using a transmitted reference and energy detection. Fourth, as an alternative to receiver-centric structure, time reversal is proposed in the transmitter-centric framework. In a sense, time reversal can be viewed as moving the channel-matching RAKE filter from the receiver end to the transmitter end. Fifth, multiple antennas can be used together with time reversal. Sixth, chirp signaling is proposed by using matched filtering based waveforms. A pair of SAW devices can be an economic implementation. Chirp UWB has the good capability to solve jamming and synchronization. When compared with time reversal, the new scheme seems effective in confined metal environments—an open problem for narrowband systems. Finally, (maybe the most important), a testbed is an answer to most system issues. The awareness of the prototyping system motivates a lot of research topics. The first generation (1G) testbed is documented Chapter 4. At this time of writing, the 1G testbed is working over the air. Jointly funded by ONR, ARO, and NSF, the second generation (2G) testbed will have the time reversal capability.

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Chapter 2

Time Reversal MIMO Performance

UWB technology is generally limited to short range applications, due to the strong power limitations imposed by Federal Communications Commission (FCC). In this chapter we propose to use MIMO combined with Time Reversal (TR) technology to increase its transmission distance. The performance of such a UWB-MIMO-TR system is analyzed, considering a simple one correlator receiver. Performance comparisons are made among the scenarios of SISO-TR, MISO-TR, and MIMO-TR. The results show that a UWB-MIMO-TR system can achieve a huge power gain, depending on the antenna numbers employed at both the transmitter and the receiver, but still keeps low complexity at the receiver. The performance analysis is based on realistic channels measured in an office environment.

2.1 Introduction

Time Reversal (TR) is a technology originated from underwater acoustic and ultrasound communications[1] and has recently been extended to wireless applications [2, 3, 4, 5, 6]. Given specific time and location, TR precoding has been mathematically proved to be the optimum in the sense that it maximizes the amplitude of the field at that time and location [7]. It is then called spatio-temporal matched filter [8] because it is analogous to a matched filter both in time and space. It is also called transmit matched filter since the matched filter is placed at the transmitter side.

Considering the severe power constraints imposed on the system, the main focus of Ultra-wide Band (UWB) study has been restricted to short range applications such as communications between PCs, PDAs, cordless phones, smart appliances, and entertainment systems anywhere in and around the home. In this chapter, we propose to use multiple antennas combined with TR technology (TR-MIMO) to increase the transmission distance of pulse-based UWB systems. It should be noted that MIMO technology could either be employed to increase the data rate by decomposing the channel into a series of parallel sub-channels or to increase the signal to noise ratio (SNR), by beamforming. this chapter will mainly focus on the latter application.

TR-MIMO [9] implements MIMO directly in the time domain, and hence is believed to be much simpler, compared to those algorithms implemented in the frequency domain. However, most research on UWB-MIMO is carried out in the frequency domain, and relatively fewer results on time domain UWB MIMO have been reported. The paper [10] studies time domain MIMO and proposes to use Maximum Ratio Combining (MRC) to accomplish the temporal alignment of received pulses, which unfortunately also causes a high complexity at the receiver. By the use of TR
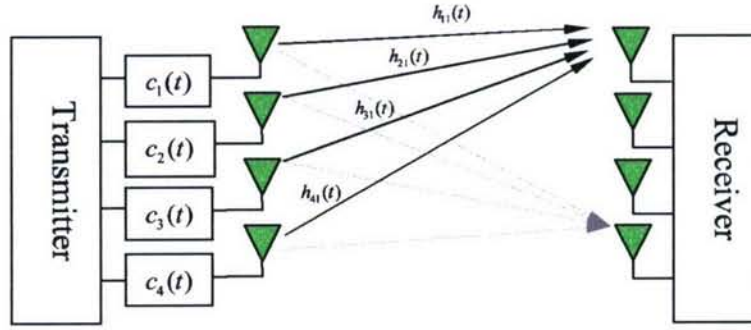
Figure 2.1: Time reversal precoded MIMO communication system with M=4 and N=4.

precoding, however, pulses are automatically aligned, and thus the receiver complexity is greatly reduced. Moreover, it is shown in [11] that TR precoding can achieve the same error performance as the MRC combining scheme.

Due to the spatial-temporally focusing of the TR technology, the energy of the received signal tends to form as a short peak. We propose to use a simple coherent receiver with one correlator to capture the main lobe energy, and treat the rest of the received signal as interference. By doing this, the receiver complexity is greatly reduced since there are no channel estimation and equalization at the receiver side. However, as we will show in this chapter, the performance of such a simple receiver can still achieve the AWGN bound under ideal conditions that all the multipath components are resolvable and there is no ISI in the system, given the same transmitted power. It is shown that a gain of $10log_{10}(MN)$ dB can be achieved by using an MIMO with M antennas at the transmitter and N antennas at the receiver.

In practice, when the pulse is short and the data rate is low, the above conditions tend to be satisfied. However, for the case of high data rate and practical pulse width, the conditions may not hold. The performance of such a practical system is investigated by Monte Carlo simulations. Considering that there is no available channel data involving multiple antennas, we carry out a series of spatial channel measurements in an office environment.

The structure of this chapter is as follows: In Section 2.2, we give the system description and the analytical performance analysis. A brief description of the experimental setup and the environment is given in Section 2.3. Some numerical results and analysis based on measurement channels are given in Section 2.4. Finally, we present the conclusions of the paper in Section 2.5.

2.2 Performance Analysis

2.2.1 MIMO-TR Precoding

An MIMO-TR (4×4) system configuration is illustrated in Fig. 2.1. Let $h_{mn}(t)$ denote the channel impulse response (CIR) between the m-th antenna at the transmitter and the n-th antenna at the receiver, and $\varsigma_n(t)$ be the corresponding prefilter code employed in the m-th antenna branch at the transmitter. In a general $M \times N$ MIMO-TR system, the code $c_m(t)$ can be written as

$$c_m(t) = A_m \sum_{n=1}^{N} h_{mn}(T-t) \tag{2.1}$$

where T is the length of the filter required to implement time reversal operation [12], and A_m is the power scaling factor to normalize the total transmission power from different antenna branches. It should be noted that different power allocation schemes can be implemented by choosing different A_m value [13]. In this chapter, for simplicity, values of A_m are set to be equal for all the antenna elements, i.e.,

$$A_m = A = \frac{1}{\sqrt{\sum_{m=1}^{M} \sum_{n=1}^{N} G_{mn}}} \tag{2.2}$$

where $G_{mn} = \int_{-\infty}^{+\infty} |h_{mn}(t)|^2 \, dt$ is the channel gain of CIR $h_{mn}(t)$.

The precoder $c_m(t)$ for the m-th antenna branch can be readily obtained by channel sounding, assuming channel is reciprocal and is static over one symbol duration. These two assumptions have been verified for UWB system by measurements in [6]. The process of MIMO-TR channel sounding includes two steps: Firstly, all N antennas at the receiver send a sounding pulse $w(t)$ to the transmitter simultaneously; Secondly, the received signal at each transmitter antenna branch is recorded, digitized and time reversed. The time reversed version of the signal in each antenna element will be used as the precoder for that antenna branch.

2.2.2 System Description

Consider a single user transmission. Transmitted signals before precoding can be expressed as

$$s(t) = \sum_{i=-\infty}^{+\infty} s_i(t) = \sum_{i=-\infty}^{+\infty} \sqrt{E_b} b_i \, p(t - iT_b) \tag{2.3}$$

where E_b is the transmitted bit energy, $b_i \in \{\pm 1\}$ is the i-th information bit. Without loss of generality, binary antipodal modulation has been considered in this chapter. $p(t)$ is the UWB pulse with a width of T_p. The energy of $p(t)$ is normalized to unity, i.e., $E_p = \int_{-\infty}^{+\infty} p^2(t) \, dt = 1$. T_b is the bit interval. Generally, we have $T_b \gg T_p$, in order to avoid the possible Inter Symbol Interference (ISI) caused by multipath channel. In this chapter, we will show that, by using a MIMO-TR technology, T_b and T_p could be chosen to be in the same level, without significant performance degradation.

For the sake of simplicity, we assume there is no per-path pulse distortion [15] caused by channel. In this case, the received signals are just a series of replicas of the transmitted signals, with different attenuations and time delays. The CIR then can be modeled as

$$h(t) = \sum_{l=1}^{L} \alpha_l \delta(t - \tau_l) \tag{2.4}$$

where L is the number of multipath components and α_l and τ_l are its individual amplitudes and delays.

2.2.3 Performance Analysis

Before we consider MIMO-TR, let us start with a simpler scenario of SISO-TR. If there is no time reversal and a single antenna is employed at both the transmitter and the receiver, the received signal can be expressed as

$$r_i(t) = \sum_{l=1}^{L} \alpha_l s_i(t - \tau_l) + n(t) \tag{2.5}$$

where $n(t)$ is Additive White Gaussian Noise (AWGN) with a two-sided power spectral density of $N_0/2$.

The optimum receiver for the above signal would be a matched filter matched to the signal part of $r_i(t)$. Such a receiver would achieve the performance bound, namely matched filter bound, described as

$$P_e = Q\left(\sqrt{\frac{2GE_b}{N_0}}\right) \tag{2.6}$$

where G is the channel gain defined in the previous section. It should be noted that the notation E_b here represents the transmitted bit energy, instead of the bit energy at the receiver side, which is noted with $\tilde{E}_b$.

In reality, it is believed that the performance bound in (2.6), requires very complex receiver and thus is hard to achieve, due to the complicated UWB multipath channel. In this section, we will show that, by using TR precoding at the transmitter, the AWGN performance bound can be achieved with a simple one correlator receiver, under some conditions.

Consider a non-realistic case where we use such a short pulse that the propagation delay difference between any adjacent multipath components is always bigger than pulse duration T_p. As suggested in the title of this chapter, we are interested in an impulse UWB case. An ideal UWB pulse will be a Delta function, an impulse with infinite short width in the time domain, or equivalently infinite bandwidth in the frequency domain. Mathematically, for an arbitrary $l \in [1, L)$, we have $|\tau_{l+1} - \tau_l| > T_p$. This assumption implies that there is no inter pulse overlap after the pulse passes through the multipath channel, which corresponds to the ideal case that all the paths are resolvable. Also we assume that T_b is large enough so that there is no Inter-Symbol-Interference (ISI).

For SISO-TR, the received signal can be expressed as

$$\begin{aligned} r_i^{SISO}(t) &= s_i(t) * c(t) * h(t) + n(t) \\ &= s_i(t) * \left\{\frac{1}{\sqrt{G}}h(T-t) * h(t)\right\} + n(t) \\ &= s_i(t) * h_{eq}^{SISO}(t) + n(t) \end{aligned} \tag{2.7}$$

where $c(t) = h(T-t)/\sqrt{G}$ is the prefilter code, and $h_{eq}^{SISO}(t) = h(T-t) * h(t)/\sqrt{G}$ is the equivalent CIR for the SISO-TR scenario. It is apparent that $h_{eq}^{SISO}(t)$ is an autocorrelation with peak occurring at $t = T$. The magnitude of the peak is equal to $\sqrt{G}$, i.e., $h_{eq}^{SISO}(t = T) = \int_{-\infty}^{+\infty} |h(t)|^2 \, dt/\sqrt{G} = \sqrt{G}$.

Due to its autocorrelation nature, most of the energy is focused in the central (main) peak of the CIR $h_{eq}^{SISO}(t)$. Since we assume there are no Inter Pulse Interference (IPI), ISI and pulse distortion, we can use a filter matched to the main component of the received signal. The following is to prove that even using such a simple receiver (with one correlator), we can achieve the same performance as the matched filter bound.

Performance analysis based on transmit bit energy E_b

For SISO-TR, the main component of the receiving signal can be expressed as

$$r_i^{main}(t) = \sqrt{G}\sqrt{E_b}b_i p(t - iT_b - T) \tag{2.8}$$

we then use a filter matched to $p(t)$,[1] to pick up the energy lying in the above main component of the received signal. The performance can be characterized using the following analytical formula,

---

[1] In reality, considering antenna effect in the system, $\tilde{p}(t)$ instead of $p(t)$ should be used. $\tilde{p}(t) = p(t) * h_a^{tx} * h_a^{rx}$, where h_a^{tx} and h_a^{rx} represent the impulse response of transmit antenna, receive antenna, respectively.

$$P_e^{SISO} = Q\left(\sqrt{\frac{2GE_b}{N_0}}\right) \tag{2.9}$$

where $Q(x) = \int_x^\infty \frac{1}{\sqrt{2\pi}} e^{-y^2/2} dy$ is the Q-function.

Comparing (2.9) and (2.6), it is evident that a TR system with one correlator receiver can achieve the same performance as a system without TR but with ideal matched filter. Same conclusion has been obtained by other researchers [11, 16], through different approaches, in a Pre-rake system. In the following, we will extend this result to a scenario of TR with multiple antennas.

For MIMO-TR, signal captured by the n-th receive antenna can be expressed as

$$r_i^n(t) = s_i(t) * \sum_{m=1}^{M} \{c_m(t) * h_{mn}(t)\} + n(t) \tag{2.10}$$

The beauty of TR is that all the signal peaks are automatically aligned at $t = T$, which is independent of the antenna location, channel, and antenna type [12]. In this case, all the signals captured by different antennas at the receiver can be combined directly, without additional pulse alignment process. The received signal $r_i(t)$ after combining can be expressed as

$$
\begin{aligned}
r_i(t) &= s_i(t) * \sum_{n=1}^{N} \sum_{m=1}^{M} \{c_m(t) * h_{mn}(t)\} + n(t) \\
&= s_i(t) * A \sum_{n=1}^{N} \sum_{m=1}^{M} \left\{ \left[\sum_{k=1}^{N} h_{mk}(T-t) \right] * h_{mn}(t) \right\} \\
&\quad + n(t)
\end{aligned}
\tag{2.11}
$$

The equivalent impulse response for MIMO-TR scenario is then expressed as

$$
\begin{aligned}
h_{eq}^{MIMO}(t) &= A \sum_{n=1}^{N} \sum_{m=1}^{M} \left\{ \left[\sum_{k=1}^{N} h_{mk}(T-t) \right] * h_{mn}(t) \right\} \\
&= \underbrace{A \sum_{n=1}^{N} \sum_{m=1}^{M} \left\{ \sum_{k=1,k\neq n}^{N} h_{mk}(T-t) * h_{mn}(t) \right\}}_{Interference} \\
&\quad + \underbrace{A \sum_{m=1}^{M} \sum_{n=1}^{N} \{R_{mn}(t) * \delta(t-T)\}}_{Signal}
\end{aligned}
\tag{2.12}
$$

where $R_{mn}(t) = h_{mn}(-t) * h_{mn}(t)$ is the autocorrelation of $h_{mn}(t)$. It can be seen from (2.12) that the equivalent CIR $h_{eq}^{MIMO}(t)$, mathematically, has MN^2 terms, consisting of MN autocorrelations and $MN(N-1)$ cross correlations. The peak of the autocorrelation terms will coherently add up, at the time instant of $t = T$, while the cross correlation term will add up noncoherently.

$$\kappa_{MIMO} \approx \frac{(\sum\limits_{m=1}^{M}\sum\limits_{n=1}^{N} G_{mn} + \sum\limits_{n=1}^{N}\sum\limits_{m=1}^{M}\sum\limits_{k=1,k\neq n}^{N} I_{mn,mk})^2}{2\sum\limits_{n=1}^{N}\sum\limits_{m=1}^{M}\sum\limits_{k=1,k\neq n}^{N} \nu_{mn,mk} + \sum\limits_{m=1}^{M}\sum\limits_{n=1}^{N} \nu_{mn} + (\sum\limits_{m=1}^{M}\sum\limits_{n=1}^{N} G_{mn} + \sum\limits_{n=1}^{N}\sum\limits_{m=1}^{M}\sum\limits_{k=1,k\neq n}^{N} I_{mn,mk})^2} \tag{2.17}$$

$$= \frac{\left[\bar{G} + (N-1)\bar{I}\right]^2}{\frac{2N-1}{MN}\bar{\nu} + \left[\bar{G} + (N-1)\bar{I}\right]^2}$$

For $t = T$, the magnitude of the peak of the CIR h_{eq}^{MIMO} can be approximated as

$$h_{eq}^{MIMO}(T) \approx A \sum_{m=1}^{M}\sum_{n=1}^{N} G_{mn} = \sqrt{\sum_{m=1}^{M}\sum_{n=1}^{N} G_{mn}} \tag{2.13}$$

Here "$\approx$" is used because the contributions from the cross correlation terms in the main peak have been ignored.

Signal in the main component is then written as

$$r_i^{main}(t) \approx \sqrt{\sum_{m=1}^{M}\sum_{n=1}^{N} G_{mn}} \sqrt{E_b} b_i p(t - iT_b - T) \tag{2.14}$$

Again, we use a filter whose impulse response is set to be $p(-t)$ to pick up the energy lying in the above main component, and ignore the other sidelobe energy. The error probability of such a system can be expressed using Q-function as

$$P_e^{MIMO} = Q\left(\sqrt{2\sum_{m=1}^{M}\sum_{n=1}^{N} G_{mn} E_b / N_0}\right) \tag{2.15}$$

Let $\bar{G}$ denote the average channel gain of the whole $M \times N$ channels, i.e., $\bar{G} = \frac{1}{MN}\sum\limits_{m=1}^{M}\sum\limits_{n=1}^{N} G_{mn}$, we have

$$P_e^{MIMO} = Q\left(\sqrt{2MN\bar{G}E_b / N_0}\right) \tag{2.16}$$

According to Eq. (2.16), it is straightforward that the performance of MIMO-TR depends on the following parameters: the antenna number M, N and the multipath condition (channel gain $\bar{G}$).

When $M = 1, N = 1$, the Eq. (2.16) reduces to (2.9) for SISO-TR scenario. Moreover, comparing (2.9) with (2.16) we can find that a power gain of MN can be achieved by employing M antennas at the transmitter and and N antennas at the receiver, respectively. This fact suggests that TR combined with MIMO can be used to extend the system transmission distance.

Performance analysis based on receiving bit energy $\tilde{E}_b$

The above analysis is based on the bit energy E_b at the transmitter side. Considering a lot of researchers analyze the performance based on $\tilde{E}_b$, bit energy measured at the receiver side, we also derive the performance formula for

$\tilde{E}_b$. It should be noted that one correlator receiver proposed in this chapter is not optimum. Instead, the optimum receiver should be a matched filter matched to the whole receiving waveform. The performance bound for such a receiver would be the matched filter bound, expressed as $P_e = Q(\sqrt{\frac{2\tilde{E}_b}{N_0}})$.

We introduce a new metric, peak energy ratio κ, defined by $\kappa = \frac{E_{peak}}{\tilde{E}_b}$, denoting the ratio of the main lobe energy to the whole receiving bit energy . The performance of one correlator receiver then can be expressed with κ as $P_e = Q(\sqrt{\frac{2\tilde{E}_b \kappa}{N_0}})$.

Let $\nu_{mn,ij}$ represent the sidelobe power of the equivalent impulse response $h_{mn,ij}(t)$. We define

$$\nu_{mn,ij} = \int_{-\infty}^{+\infty} |h_{mn}(-t) * h_{ij}(t)|^2 \, dt - I_{mn,ij}^2 \tag{2.18}$$

for unintended CIRs ($m \neq i$ or $n \neq j$), and $\nu_{mn,ij} = \nu_{mn} = G_{Rmn} - G_{mn}^2$ for intended CIRs ($m = i$ and $n = j$). Here

$$I_{mn,ij} = |h_{mn}(-t) * h_{ij}(t)|_{t=0} = \int_{-\infty}^{+\infty} |h_{mn}(t) \times h_{ij}(t)| \, dt \tag{2.19}$$

and

$$G_{Rmn} = \int_{-\infty}^{+\infty} |R_{mn}(t)|^2 \, dt \tag{2.20}$$

is the channel gain of the equivalent CIR $R_{mn}(t)$.

For MIMO-TR, the peak energy ratio κ_{MIMO} can be expressed as Eq. (2.17).

In Eq. (2.17), the bar notation $\bar{(.)}$ represents an averaging operation, i.e.,

$$\bar{G} = \frac{1}{MN} \sum_{n=1}^{N} \sum_{m=1}^{M} G_{mn} \tag{2.21}$$

$$\bar{I} = \frac{1}{MN(N-1)} \sum_{n=1}^{N} \sum_{m=1}^{M} \sum_{k=1, k\neq n}^{N} I_{mn,mk} \tag{2.22}$$

and

$$\bar{\nu} = \frac{1}{MN(2N-1)} \{ 2 \sum_{n=1}^{N} \sum_{m=1}^{M} \sum_{k=1, k\neq n}^{N} \nu_{mn,mk} + \sum_{m=1}^{M} \sum_{n=1}^{N} \nu_{mn} \} \tag{2.23}$$

In reality, if the antenna elements are placed far enough so that there is no correlation among the CIRs, the value of $I_{mn,ij}$ is very small and could be ignored. Then we have

$$\kappa_{MIMO} \approx \frac{\bar{G}^2}{\frac{2N-1}{MN}\bar{\nu} + \bar{G}^2} \tag{2.24}$$

For large N, Eq. (2.24) can be approximated by

$$\kappa_{MIMO} \approx \frac{\bar{G}^2}{\frac{2}{M}\bar{\nu} + \bar{G}^2} \tag{2.25}$$

For MISO-TR

$$\kappa_{MISO} \approx \frac{(A \sum\limits_{m=1}^{M} G_m)^2}{A^2 \sum\limits_{m=1}^{M} \nu_m + (A \sum\limits_{m=1}^{M} G_m)^2} = \frac{\bar{G}^2}{\frac{1}{M}\bar{\nu} + \bar{G}^2} \tag{2.26}$$

For SISO-TR

$$\kappa_{SISO} = \frac{G^2}{\nu + G^2} \tag{2.27}$$

As a sanity check, when $N = 1$, (2.24) reduces to MISO case (2.26), and for $M = 1$ and $N = 1$, (2.24) reduces to SISO case (2.27).

It is evident from (2.25) and (2.26) that the performance of both MIMO and MISO depends on the number of transmit antenna M. If we increase M, we actually improve the focusing and then get better performance. Overall, In terms of κ, MISO outperforms MIMO, especially when N is large, the κ improvement caused by increase of M for an MISO is much faster than that of an MIMO. This has been verified by our measurement, as will be illustrated by Table 2.1 in the following section.

2.3   UWB Spatial Channel Measurement

Considering that there is no available channel model with multiple antennas available so far, we conduct a series of measurements in an office environment. A virtual antenna array is employed in the experiments. The elements of the array are spaced far enough such that there is no coupling between them. Line of Sight (LOS) is not available for all the measurements. The environment for the experiment is a typical office area with abundance of wooden and metallic furniture (chairs, desks, bookshelves and cabinets). A detailed experiment setup and environment description can be found in [12].

A (4×4) virtual MIMO array, corresponding to 16 SISO channels and 4 (4×1) MISO channels, were measured in our experiment campaign. A typical received waveform and its corresponding CIR are shown in Fig. 2.2. The CLEAN algorithm [14] is employed to extract CIR from the received waveform.

Based on the measured CIRs, comparisons of κ among different scenarios are given in Table 2.1. In Table 2.1, $T_m R_n$ denotes the channel between the m-th transmit antenna and the n-th receive antenna. The parameters ν and G are directly measured from the equivalent CIRs of different channels. For SISO-TR, the parameter κ is calculated using (2.27), while for MISO-TR and MIMO-TR, we have two approaches to calculate the value of κ. The approximated values are calculated using (2.25) and (2.26), while the experimental values are exact values calculated directly based on their equivalent CIRs. It can be seen that approximated values and experimental values are very close, implying our approximations are valid.
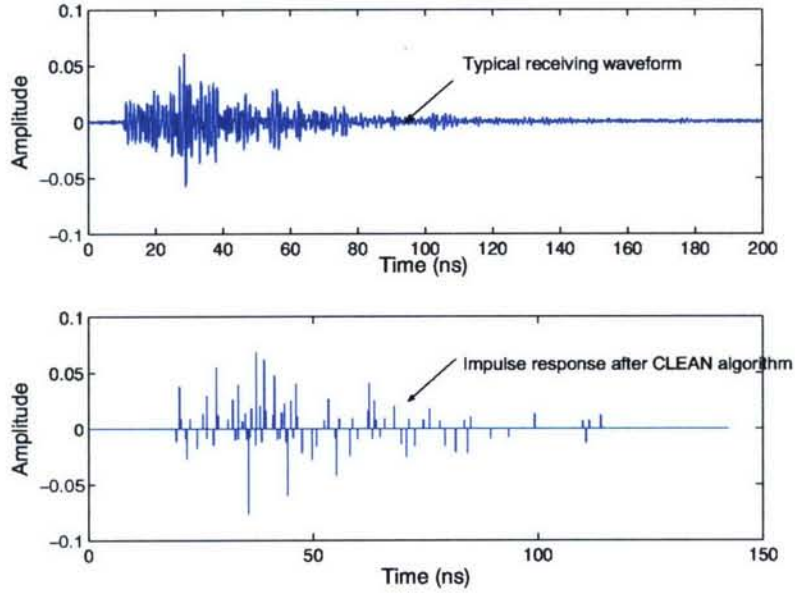
Figure 2.2: Channel impulse response extracted with CLEAN Algorithm

2.4 Numerical Result

In our simulation, the second order derivative of Gaussian pulse has been used as the transmitted pulse $p(t)$, which is mathematically defined as:

$$p(t) = \left[1 - 4\pi \left(\frac{t - t_c}{w}\right)^2\right] e^{-2\pi \left(\frac{t - t_c}{w}\right)^2} \tag{2.28}$$

where w is the parameter controlling the width of the pulse (and therefore the frequency bandwidth of the transmit signal), and t_c is the parameter to shift the pulse to the middle of the window. In the following simulation, we let $w = 1 \ ns$ and $t_c = 0.5 \ ns$. To avoid the presence of severe ISI in the system, we add a inter-pulse guard time T_g. Therefore, we have $T_b = w + T_g$. Moreover, T_g can be used to adjust the transmission data rate. Unless stated otherwise, we let $T_g = w$, corresponding to a data rate of 500 Mb/s.

Throughout of the paper, we assume perfect synchronization and the transmitter has the full knowledge of the channel information. Under these assumptions, we conduct Monte Carlo simulations to investigate the performance of one correlator receiver and compare them under different scenarios: SISO, MISO, and MIMO.

To make the comparison fair, performance of SISO and MISO scenarios have been averaged over all the corresponding specific channels that form the MIMO channel, i.e., $P_{ave}^{SISO} = \frac{1}{16} \sum_{i=1}^{16} P_i^{SISO}$, and $P_{ave}^{MISO} = \frac{1}{4} \sum_{i=1}^{4} P_i^{MISO}$.

First let us consider a system without ISI and IPI. The performance of one correlator receiver can be characterized with Q-function as $P_e = Q(\sqrt{\frac{2\tilde{E}_b \kappa}{N_0}})$. Fig. 2.3 shows a comparison of BER performance among SISO, MISO, and MIMO scenarios, based on receiver SNR $\tilde{E}_b/N_0$. The values of κ are obtained from Table 2.1. From Fig. 2.3 we can see that, given the same SNR at the receiver side, MISO-TR has the best performance. This is due to the best temporal focusing provided by MISO-TR. A comparison of BER performance with ISI and IPI is shown in Fig. 2.4.
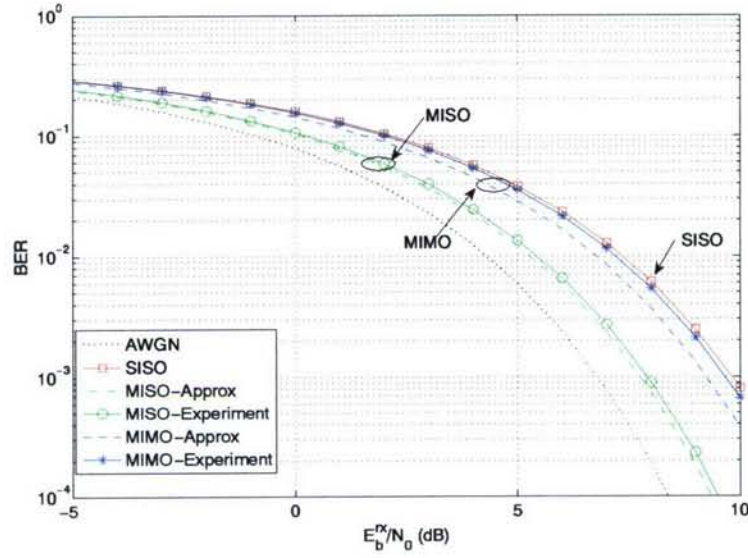
Figure 2.3: BER performance based on the bit energy at the receiver side, assuming there are no ISI and IPI.

The performance bound for AWGN channel is also plotted as a reference. It should be noted that the comparisons in Fig. 2.3 and 2.4 are based on the same received SNR. In reality, however, given the same transmitted power, the SNR at the receiver side for MIMO-TR is much higher than that of MISO-TR, which makes MIMO-TR outperform MISO-TR. In the following, we compare the performances for different scenarios based on same total transmit (total) power constraint.

Fig. 2.5 shows the BER performances for the SISO, MISO , and MIMO scenarios, based on transmitter bit energy, with different transmission data rates. Both IPI and ISI have been considered. As we can see from Fig. 2.5, MIMO-TR outperforms MISO-TR and then MISO-TR outperforms SISO-TR. Tests were conducted for data rates of $500Mb/s$ and $225Mb/s$. As expected, A increase in the data rate leads to a degradation performance. For a data rate of 250 Mb/s, about 13 dB power gain is achieved by employing a 4×4 MIMO array. The power gain with ISI and IPI is slightly higher than the theoretical power gain $10log_{10}(MN)$, derived in Section 2.2, where we assume there are no ISI and IPI.

2.5   Conclusion

We evaluate the performance of UWB-MIMO-TR system, considering a simple one-correlator receiver. Performance comparisons among different scenarios, namely, SISO-TR, MISO-TR, and MIMO-TR are provided, based on both the transmitted bit energy and the received bit energy. The results show that a power gain of MN could be achieved with a system of MIMO-TR. The gain becomes even larger, if both ISI and IPI are considered, due to the MIMO-TR has better temporal focusing.

It should be noted that MIMO-TR is, indeed, simple, but not the optimal way. The philosophy behind time reversal is so called transmit centric processing, i.e., processing the signal at the transmitter side before transmission to combat the deteriorating effects of the channel. Transmit centric processing greatly simplifies the receiver, and is desirable
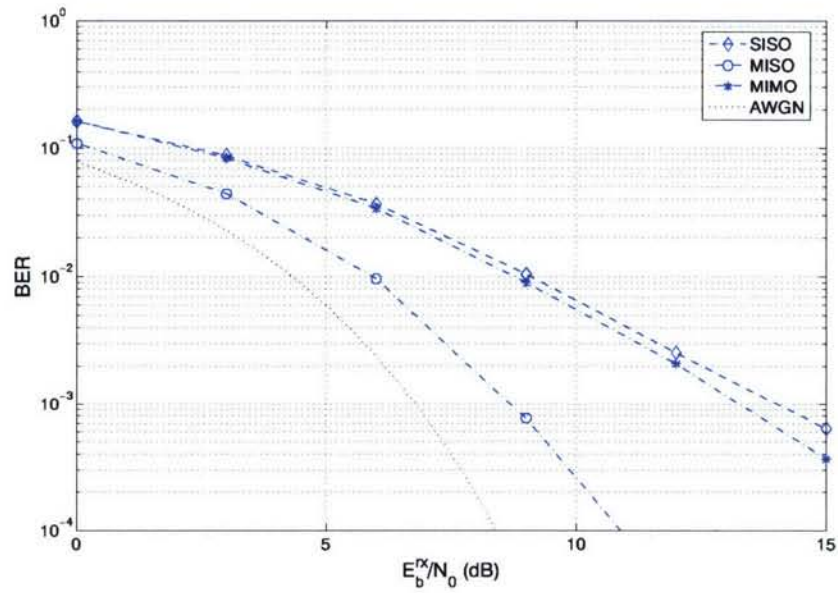
Figure 2.4: BER performance in terms of received bit energy. Both IPI and ISI have been considered.

in the case where one base station (BS) serves many mobile stations (MS).

A single user scenario has been considered in this chapter. Considering TR with multiple antennas further increases spatial focusing, thus reducing the multi-user interference, MIMO-TR should have even better performance when a multi-user (MU-MIMO-TR) scenario [17] is studied.
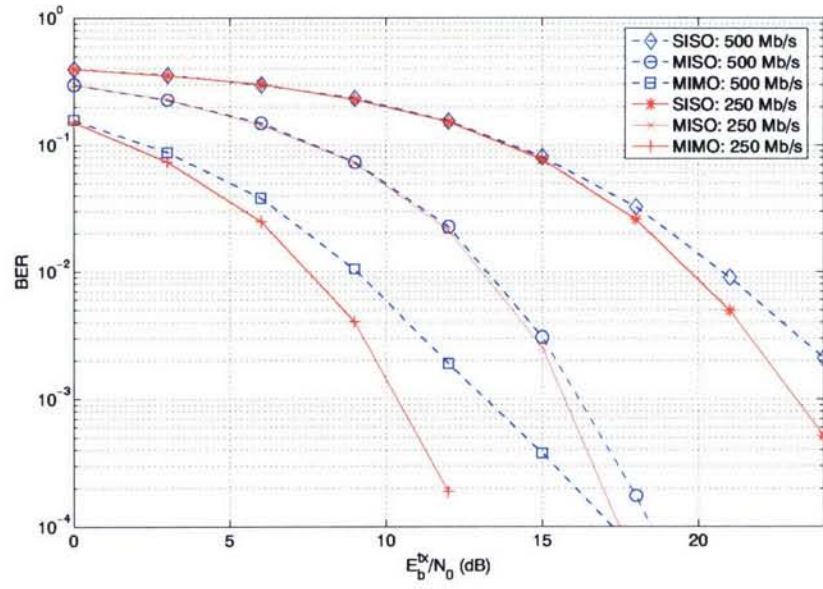
Figure 2.5: BER performance in terms of transmitted bit energy. Both ISI and IPI have been considered.

Table 2.1: A Comparison of κ for Different Scenarios

	Channel	ν	G^2	κ
	T_1R_1	0.0459	0.0483	0.5124
	T_1R_2	0.0414	0.0454	0.5230
	T_1R_3	0.0485	0.0467	0.4906
	T_1R_4	0.0572	0.0581	0.5040
	T_2R_1	0.0516	0.0512	0.4979
	T_2R_2	0.0446	0.0413	0.4810
	T_2R_3	0.0457	0.0455	0.4991
	T_2R_4	0.0556	0.0477	0.4615
	T_3R_1	0.0562	0.0543	0.4915
SISO-TR	T_3R_2	0.0363	0.0355	0.4944
	T_3R_3	0.0346	0.0367	0.5148
	T_3R_4	0.0454	0.0451	0.4983
	T_4R_1	0.0502	0.0485	0.4916
	T_4R_2	0.0462	0.0445	0.4906
	T_4R_3	0.0595	0.0573	0.4907
	T_4R_4	0.0366	0.0369	0.5020
	Average	0.0472	0.0464	0.4965
	$T_{1234}R_1$	0.0577	0.2022	*Appro:* 0.8044
				Exper: 0.7781
	$T_{1234}R_2$	0.0493	0.1663	*Appro:* 0.7900
MISO-TR				*Exper:* 0.7714
	$T_{1234}R_3$	0.0520	0.1851	*Appro:* 0.7992
				Exper: 0.7807
	$T_{1234}R_4$	0.0605	0.1865	*Appro:* 0.7955
				Exper: 0.7552
	Average	0.0549	0.1850	*Appro:* 0.7977
				Exper: 0.7713
MIMO-TR	$T_{1234}R_{1234}$	0.6401	0.6781	*Appro:* 0.5680
				Exper: 0.5144

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Chapter 3

Design Consideration of Transceiver Technology for Second Generation (2G) Testbed

3.1 Unique Features and Issues

The work of a transceiver designer is to provide a feasible solution under some theoretical and practical criteria. A very broad range of issues need to be considered. Here just name a few: frequency and band, architecture, data rate, modulation, synchronization, coexistence, interference suppression/cancellation, implementation, etc. For indoor UWB radio, the fact of rich and resolvable multipath with low fading enables unique capabilities and features such as ranging with sub-foot accuracy, small link-budget margin, quasi-stable channel and precoding. LPI/LPD is automatically achieved from the nature of UWB radio's low power spectral density, and traditional spread spectrum techniques can be used to enhance the LPI/LPD feature further.

3.2 Why Suboptimal Receivers?

On the other hand, rich multipath channel characteristic poses a number of challenges to system design and implementation. Traditional RAKE receiver that maximizes receive SNR is not a proper solution since tens of fingers have to be implemented to capture enough energy. OFDM is another "optimum"-achieving scheme but it is not a cheap solution either. With constraints of complexity, power consumption and cost, we should find some alternative transceiver schemes that trade performance for reduced complexity. The optimal receivers highly depend on fine synchronization and channel estimation, while the suboptimal counterparts, such as transmitted reference (TR) and energy detector schemes, are not quite sensitive to timing error and do not require channel estimation at all.

3.3   Interference and Jamming Issues

Operating over wide frequency bands of at least 500 MHz, a UWB system has good chance of suffering from unintentional interference and intentional jamming. Filter bank, notch filter and spread spectrum are always good candidates for interference suppression/cancellation. In contrast to some conventional interference suppression/cancellation methods, multiple antennas can take advantage of UWB's scattering propagation to achieve signal focusing or nulling spatially, opening a new dimension for handling the interference and jamming issues.

3.4   Synchronization

Initial timing acquisition is one of the most important and difficult parts in the system. Note that non-coherent receivers can make initial timing acquisition more difficult due to loss of polarization information after the detector. This difficulty translates to a longer synchronization preamble and a longer package synchronization time. It is still an open issue to find a proper acquisition strategy and to optimize the algorithm. So far a two-stage acquisition algorithm based on the optical orthogonal code (OOC) has been designed and tested in our testbed.

3.5   Multi-Antenna Precoding

Precoding is a transmitter-side signal processing technique that can efficiently compensate channel propagation impairments to achieve some system design goals. Precoding has a few advantages over receiver-side signal processing schemes like equalization and RAKE combining. One major benefit of precoding is that part of the system complexity is shifted from the receiver to the transmitter, which is greatly meaningful to some centralized network with large number mobile nodes. Transmitter-side processing solely affects the signal and has no impact on the noise, unlike some equalization (at the receiver) that may amplify the noise power. There are many precoding design criteria, including water filling for maximum capacity, cross talk cancellation, spectrally nulling and ISI reduction. However, precoding requires that the channel impulse response (CIR) is known and static in an observation time window. Study has shown that the UWB channels can be very static, and channel reciprocity has also been verified by our experiments.

At GHz frequency level centimeter-size antennas can be designed, and it is not difficult to obtain a compact antenna array with negligible spatial correlation between antenna elements. An antenna array at transmitter side can be nicely combined with some precoding to maximize performance without requiring sophisticated receivers. Illustrated in Fig.3.1 is a multiple input single output (MISO) precoding configuration, where $c_n(t)$'s represents precoders and $h_m(t)$'s are CIRs.

3.6   Multiple-Access

Multiple-access is about how to separate multiple users using some orthogonality mechanism. Low-complexity multiple-access is badly demanded for low-cost applications such as sensor networks. In stead of using time, frequency or code resources, spatial division multiple access (SDMA) is a more spectrally efficient method. A down-
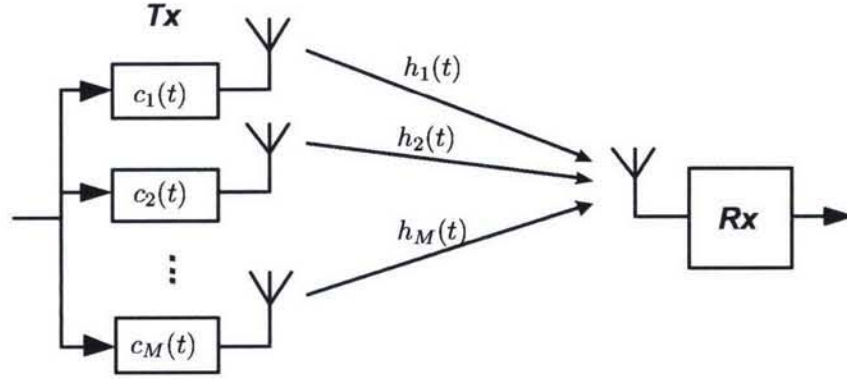
Figure 3.1: MISO precoding configuration.

link SDMA technique enabled by MISO time reversal has been examined using our indoor measured data [29]. It takes advantage of rich multipath to focus signal spatially and separate users.

In addition, a time-of-arrival (TOA) based multiple access technique has been proposed in [1] specifically for up-link low duty-cycle pulsed signaling. The proposed multiple-access method is based on a phenomenon called multiple delay capture [2]-[5]. This is a random multiple-access that can be viewed as TOA division multiple-access, and its performance depends on the probability that signals collide (or overlap) at the receiver. To reduce the chance of collision, MISO time reversal is considered to condense the UWB channel impulse response (CIR).

3.7   Nonlinear Discrete Channels with Memory

Unlike linear receiver, the equivalent discrete channels of some suboptimal schemes behave nonlinearly, where an equivalent discrete channel has data input and outputs decision statistic plus noise. For both differential TR (ACD) and energy detection, their equivalent discrete channels can be modeled as [28][28][29]

$$z_k = \vec{d}_k^T C \vec{d}_k + \eta_k, \tag{3.1}$$

where $\vec{d}_k$ is a vector of data, C is a matrix determined by the channel, and η_k is a noise term. This means that the signal part in the output of the equivalent discrete channel, i.e., $\vec{d}_k^T C \vec{d}_k \overset{def}{=} S_k$, is a nonlinear function of data vector $\vec{d}_k$. As a matter of fact, the equivalent discrete channel represented by $S_k = \vec{d}_k^T C \vec{d}_k$ is a special case of second-order Volterra model [23][31]. In general, z_k contains a desired signal and a nonlinear inter-symbol-interference (ISI) component that cannot be well handled by normal linear equalization techniques, which motivates our work on transmitter-side signal processing.

3.8   System Architecture and Implementation

OOK modulation with energy detector is a reasonable combination for low cost applications. The baseband functions are implemented using FPGA in the testbed. The embedded system (DSP chip) is also a good candidate for baseband

processing, but FPGA platform has potential to support much higher data rate (up to Gb/s). In order to have more flexibility in exploring different receiver schemes and signal processing algorithms on the testbed, the analog-digital partitioning line at the receiver is set at the output of the energy detector.
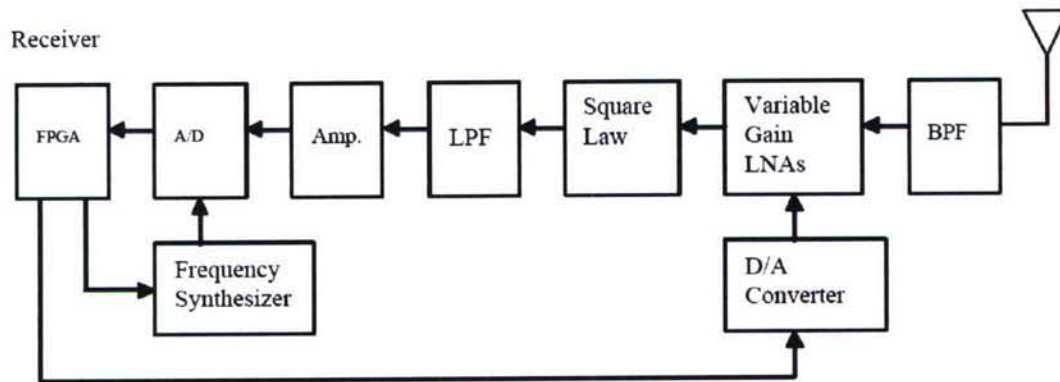
Figure 3.2: Receiver architecture.

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Chapter 4

Testbed Development

This chapter describes the first generation (1G) testbed developed at TTU. The second generation (2G) is under development. The 1G system uses an energy detection transceiver that shoots for low-cost and low power applications. The 2G system will use time reversal that has higher complexity, but has much better performance. As pointed out before, time reversal can be viewed as moving the generalized RAKE from the receiver side to the transmitter side. The complexity is, thus, moved to the transmitter side. The 2G testbed is built on the 1G hardware.

4.1 Introduction

In 2002 the Federal Communication Commission (FCC) allocated limited use of a huge chunk of spectrum between 3.1 GHz and 10.6 GHz to allow UWB systems overlaying over existing narrow-band systems. Since then the tremendous potential has triggered great interest in both academia and industry. Industrial standards such as IEEE 802.15.3a (for high data rate) and IEEE 802.15.4a (for low data rate with ranging) using UWB band have been introduced. Among many proposed UWB systems for IEEE 8092.15.3a are two major proposals: the Multi-Band OFDM Alliance (MBOA) proposal and the direct-sequence UWB (DS-UWB) proposal. The MBOA system employs orthogonal frequency-division multiplexing (OFDM) modulation to solve the severe multipath problem. On the other hand, the DS-UWB system uses direct-sequence spread-spectrum technology and relies on the RAKE receiver to capture signal energy dispersed over a large number of paths. The both systems may give high performance, but they are not low-cost solutions at present.

In contrast, suboptimal alternatives targeting at low-cost wireless applications, such as sensor networks, have received great attention [21] [22] [26] [27] [29] [32] [50]. The price point will be in the sub-$1 range for asset tracking and tagging, up to $3 to $4 per node for industrial-control applications. These suboptimal solutions include transmitted reference (TR)[21] [22] [26] [27] and energy detection using a square law detector [29] [32] [50].

To research these new concepts unique to UWB, theoretical and simulation approaches are not sufficient. It is desired to use experimental ways to test schemes and algorithms, verify theoretical and simulation results, and remove some uncertainties caused by channels, hardware and software. A testbed would be very convenient to evaluate the pros and cons of some specific system aspects, such as modulation schemes, receiver structures, and the analog-to-digital (A/D) converter, etc. In particular, the experimental approach is usually the only effective means to find the actual impacts of radio frequency (RF) circuits, including antennas.

4.2   Major System Design Considerations

Implementing UWB transmitters and receivers poses a number of challenges. The difficulties mainly come from generating, transmitting and processing the very high-bandwidth signal. Major design considerations are discussed in this section.

4.2.1   Pulse Generator

Because of the minimum bandwidth requirement (-10 dB bandwidth greater than 500 MHz or -10 dB fractional bandwidth greater than 20%) and the Part 15 power limit (maximum equivalent isotropic radiated power spectrum density of -41.25 dBm/MHz), efficient use of a piece of UWB spectrum is a big challenge. The MBOA system relies on multiple subcarriers to achieve desired overall signal spectrum. On the other hand, pulse based UWB schemes are attractive for low-cost low-data-rate communication and ranging applications. The spectral content of pulse waveforms is highly dependent on the shape of the pulse generated, which makes pulse design more challenging. There have been a number of proposals of pulse generators. A simple way is to upconvert a baseband pulse to an RF center frequency. It has been proposed to use root raised cosine baseband (RRC) pulse shape for the DS-UWB system.

4.2.2   Modulation Schemes and Receiver Strategies

A direct consequence of a high-bandwidth UWB signal is ultra fine multipath delay resolution in multipath propagation environments. Theoretically, to efficiently capture the signal energy dispersed over a large number of individual paths, either a RAKE receiver scheme or an OFDM scheme can provide high performance, given perfect synchronization and channel estimation. Realistically, a RAKE receiver with tens of fingers is infeasible, and both schemes mentioned above are financially improper for low-cost low-data-rate applications. There is a huge potential market for these lower-end applications, such as sensor networks. In response to this need, several suboptimal receiver schemes, including TR and energy detection using a square law detector, have regained popularity in the UWB community [21] [22] [26] [27] [29] [32] [50]. Although both TR and energy detection suffer from performance penalty, they have no need for sophisticated channel estimation and precise synchronization, which significantly reduces receiver complexity and cost. On-off keying (OOK) modulation and energy detection is indeed a reasonable combination. Received signal energy can be captured easily using a diode (square law) detector followed by an integrator, and OOK works fine if the data symbol boundary is roughly known and inter-symbol-interference (ISI) is negligible. Pulse position modulation (PPM) is another popular modulation for pulse based UWB systems, and high order PPM or called M-ary PPM is promising to work with channel coding to achieve wide range of scalability.

4.2.3   Synchronization

Synchronization is a common issue for all types of communication systems and there have been many proposed strategies for initial timing acquisition and tracking during communication. For pulse based UWB radio, signal acquisition is extremely difficult since the pulses are often very narrow (say, 1 ns) and run at very low duty cycles. Timing is relaxed for demodulating signal of OOK format, but at least symbol boundary has to be roughly known. Energy detection employed in our testbed is one of non-coherent demodulation schemes which are not able to

identify signal polarity. One challenge for any non-coherent receiver is that initial acquisition has to rely on a uni-polar sequence (e.g., the Baker code) whose autocorrelation is typically less sharp than that of a bi-polar sequence (e.g., the m-sequence). It has been found that in multipath case the uni-polar sequence works poorly, especially when ISI occurs. In addition, non-zero-mean noise at the output of the detector, an inherited disadvantage of a non-coherent receiver, makes decision more difficult. To ensure acceptable probability of detection given certain probability of false alarm, the search needs longer time compared to the approaches for conventional systems. Some commonly used search strategies, such as multi-stage search [51], can be adopted to improve acquisition performance.

4.2.4 Other Issues

Co-existence and anti-interference

The UWB spectrum is shared with other systems and one major problem is the mutual interference between the UWB and WiFi systems. From a physical layer design point of view, traditional countermeasures to achieve capability of co-existence and anti-interference include spread spectrum and interference cancellation. For non-coherent receivers, frequency hopping (FH, one of spread spectrum techniques) can be considered, where the mutual interference is reduced by a factor of the processing gain. Notch filter is another effective means which is simpler but less flexible than FH.

Spectral Spikes

This is a problem unique for OOK and PPM modulation schemes. Owing to unbalanced modulation, lines would appear over the spectrum of the RF signal. Without proper means to reduce the spectral spikes, signal power has to be backed up to prevent from violating the FCC power limit. Pseudonoise (PN) code scrambling is a normal way to balance the signal in time domain statistically and smooth the spectrum. The scrambling method can be in the manner of direct-sequence spread-spectrum (DS/SS) or time hopping (TH).

Multiple User Access

Carrier sense multiple access/collision detection (CSMA/CD) is a popular random multiple access protocol that is suitable for a network with relatively low traffic load. Other candidates include pulling, code division multiple access (CDMA), and hybrid protocols. Recently a rate division multiple access (RDMA) scheme that takes advantage of low duty cycle of pulse based UWB signaling was proposed [52]. Because of the low duty cycle manner, users with different transmit rates can be supported at low probability of collision.

Adaptive threshold

the decision threshold has a great impact on the performance of the energy detection receiver. A good threshold can be determined by using some channel quality indicator and feedback information provided by the digital processor (back-end) at the receiver.

Data Format and Scalability

Research has showed that the UWB channels are relatively stable compared to narrow band channels, which implies that a large packet with limited control bits in the head followed by pure information bits can be used. Scalability is highly desired since application and propagation environment change dynamically. A wide range of data rates need to be supported through using different combinations of modulation, channel coding and spread spectrum.

4.3   Testbed Design

The main goal is to build a pair of concept-proof transmitter and receiver to test and verify various schemes. The testbed is expected to be flexible enough to accommodate several major transmission and reception techniques. The strategy is to develop the testbed based on our latest research work and use commercially available off-the-shelf components to expedite the project.

4.3.1   System Design

The baseline testbed is expected to accommodate the following functions/capabilities: (1) efficient pulse generation methods; (2) enabling investigation of A/D technologies such as mono-bit; (3) experimental evaluation of radio RF circuitry impact; (4) different modulation schemes, OOK, PPM and PAM; (5) test of various signal processing algorithms; (6) interface with multimedia (video, audio, etc). Several specific parameters of the baseline testbed are as follows:

- Center frequency: 3.5 - 4.0 GHz

- Bandwidth: ≥ 500 MHz

- Distance: up to 30 m

- Pulse repetition frequency: up to 20 MHz

The transmitter and receiver architectures are illustrated in Fig. 4.1. The transmitter uses an upconverter based pulse generator. The receiver relies on one or two diodes to implement square law operation. Following the diode detector is a low-pass filter which enables use of relatively lower sampling frequency. Amplifier gain and required dynamic range are key parameters that affect RF front-end design, and they can be determined with consideration of the Part 15 limit, distance range and raw data range, etc. The field programmable gate array devices (FPGAs) serve as digital back-end playing signal processing functions. Advanced AGC and adaptive thresholding are accommodated based on digital signal processing. Several key parameters of the transmitter and receiver, such as center frequency, amplifier gain, A/D converter's sampling rate and resolutions (from 1 to 8 bits), pulse repetition frequency (PRF) and data rate, are programmable.

Depending on the propagation environments, either the Barker code or the optical orthogonal codes (OOC) [53] are used for initial timing acquisition purpose. The OOC codes can be much longer than the Barker code and exhibit better autocorrelation property, which is desired for severe propagation cases.

Finally, the link budget result is shown in Table 4.3.1, where a 4GHz center frequency is assumed.

TABLE 4.3.1 Link budget.

Parameters	Values
Raw bit rate Rb	500 kbps
Average Tx power	-15 dBm
Tx antenna gain	0 dBi
Center frequency	4 GHz
Path loss at 1 m	44.48 dB
Path loss at 30 m	74.03 dB
Rx antenna gain	0 dBi
Average Rx power	-89.03 dBm
Thermal noise power per bit: $-174 + 10 * log10(R_b)$	-117.01 dBm
Noise figure	7 dB
Total noise power per bit	-110.01 dBm
Minimal required E_b/N_0	12 dB
Implementation loss	4 dB
Link margin	4.98 dB
Proposed minimal Rx sensitivity	-94.01 dBm

Figure 4.1: Transmitter and receiver architectures.

4.3.2 Board Level Design

Board level design is guided by the system design. Major issues with respect to implementation are discussed in the following.

Selection of Antennas

Generally, a small-size omni-directional antenna with voltage standing wave ratio (VSWR) $\leq$ 2 is a reasonable choice. The antennas selected are a pair of omni-directional print antennas. The antenna gain is about 2 dBi at 4 GHz, and it exhibits a voltage standing wave ratio (VSWR) $\leq$ 2 for a frequency range of 3.1 - 10.0 GHz.

Pulse Generator

Upconverter based pulse generator is used. The baseband pulse is generated using digital logic circuitry. The width of the baseband pulse, or equivalently, the signal bandwidth, is controlled by the FPGA, and the pulse strength is adjusted to meet the mixer's requirement. To flexibly generate a wide range of frequencies, a phase lock loop (PLL) based frequency synthesizer with an external loop filter and voltage controlled oscillator (VCO) serves as the local oscillator (LO). The frequency synthesizer can support frequency up to 6 GHz, the bandwidth of the loop filter is 50 kHz, and the averaged tuning sensitivity of the used VCO is 62 MHz/V. A double balanced mixer followed by a bandpass filter is used to shift the baseband signal to an RF signal. The designed local oscillator generates output frequencies with 10 MHz channel separation from 3.5 GHz to 4.0 GHz. Several filters are placed at the transmitter front-end to improve the overall transmitted signal spectrum.

Variable Gain Power Amplifier

A power amplifier in conjunction with a variable attenuator serves as the variable gain power amplifier. The overall gain is from -11 dB to +12 dB controlled by an analog signal. The control signal comes from the digital back-end through a digital-to-analog (D/A) converter with 10 bits resolution and 1.2 V reference voltage.

Variable Gain Low Noise Amplifier (LNA)

A variable gain LNA is combined using several LNAs and a variable attenuator. The gain range is from 55 dB to 70 dB considering the desired received power range and the input voltage range required by the diode detector. The overall gain in the receiver RF chain is controlled by the digital back-end through an AGC feedback loop.

Programmable A/D Converter

An 8-bit monolithic bipolar A/D converter with sampling rate up to 1.5 Gbps is selected. A high-frequency clock synthesizer is used to generate the sampling clock for the A/D converter. The variable sampling rate is achieved by controlling the output frequency of the clock synthesizer. The A/D converter features an on-chip, selectable 8:16 output demultiplexer. A double-data-rate (DDR) interface implemented in FPGA connects the A/D converter to the FPGA. Although the maximal resolution is 8 bits, lower resolution can be chosen in signal processing.

Diode Based Square Law Detector

A surface mount schottky diode with sharp I-V slope and small capacitance is used as the square law device. Following the diode is a low-pass filter which enables use of relatively lower sampling frequency, and a baseband amplifier to interface with the A/D converter.

FPGA

The Xinlix Virtex-II FPGA family is considered for the digital back-ends for both of the transmitter and receiver. The Virtex-II family is a popular platform of FPGA based on IP cores and customized modules, and is suitable for wireless applications. The model selected is XC2V1000 corresponding to one million system gates which is sufficient for the testbed needs.

Signal Processing Algorithms

A large number of digital signal processing and controlling functions need to be implemented in the digital back-ends (FPGAs). The FPGA design block diagrams for the transmitter and the receiver are shown in Fig. 4.2 and Fig. 4.3, respectively. Listed below are most basic functions at the transmitter and the receiver.

Transmitter:

- Controller and interface

- Modulation

- Coding

Receiver:

- Controller and interface

- Synchronization

- Demodulation

- Decoding

- AGC

- Automatic thresholding

Figure 4.2: Transmitter FPGA block diagram.

4.4   Testbed Prototyping

A pair of UWB transmitter and receiver with limited functions has been built and tested in the Wireless Networking Systems Laboratory. It is a complete end-to-end UWB communication system. The system working range is up to 4 meters. No AGC loop is implemented in the receiver. On-Off keying is chosen as the modulation scheme. No equalization is considered. The implementation of the ranging algorithm is not included in the testbed.

Several specific parameters of the testbed are as follows:

- Center frequency: 4.0 GHz

- Bandwidth: 500 MHz

- Data rate: 1.5625Mbps

- Pulse repetition frequency: 6.25MHz

- Distance: 4 m

- Modulation: OOK

Figure 4.3: Receiver FPGA diagram.

4.4.1 Testbed Configuration

The architecture of the transmitter and the receiver is shown in Fig. 4.1. Illustrated in Fig. 4.4 is the testbed configuration. In order to reduce the development cycle, the RF board and FPGAs are not integrated into a single printed circuit board. The FPGA development board, MEMEC DS-BD-V2MB1000, serves as the digital back-end playing signal processing functions in both of the transmitter and the receiver. The FPGA device on the development board is xc2V1000, one Xilinx product of Virtex II platform. The FPGA devices are configured by Xilinx software IMPACT via a xilinx programming cable, parallel cable IV. In the transmitter, the RF board is plugged in the expansion port JX1 on the FPGA development board. The evaluation board MAX108EVKIT for an ultra-high speed ADC MAX108 from Maxim Integrated Products serves as ADC in the receiver. The output signal of the square law detector is fed into the ADC board via a 50 Ω coaxial cable with SMA connector. An external sampling clock is required by the ADC board. It is generated by the signal generator SMIQ03B from Rohde Schwarz. The digital output of the ADC board are sent to the FPGA board for signal processing.

Figure 4.4: Testbed configuration.

4.4.2   ADC Board and High-speed Interface

The MAX108 evaluation board is used to perform the analog-to-digital conversion. The differential signaling is required for the input analog signal and sampling clock. The sampling rate is up to 1.5GSPS which is determined by frequency of the external sampling clock. A sinewave with power of +4dBm generated by the signal generator SMIQ03B is fed into the CLK+ port on the ADC board as the sampling clock. The CLK- port on the ADC board is grounded via a 50 Ω SMA terminator. The input analog signal is connected to the port VIN+ on the ADC board through a 50 Ω SMA coaxial cable. The VIN- port on the ADC board is grounded vis a 50 Ω SMA terminator. Since the input signal range of the ADC board is from -250mV to +250mV, a 10dB passive attenuator is placed between the output of RF board and the input of the ADC board. The ADC resolution is 8 bits. The MAX108 evaluation board has demultiplexed differential PECL outputs. Total 16 pairs of PECL output signals are connected to the FPGA development board. The frequency of the output signal is reduced to the half frequency of the sampling clock. The most significant 4 bits of ADC output are used in the FPGA design in order to achieve the balance between performance and complexity.

For the design of the high-speed interface between ADC and FPGA, signal integrity has become a critical issue. Many signal integrity problems are electromagnetic phenomena in nature and hence related to the EMI/EMC. There are two concerns for signal integrity - the timing and the quality of the signal. Signal timing mainly depends on the delay caused by the physical length that the signal must propagate. Signal waveform distortions can be caused by reflection, cross talk and power/ground noise. An interface board must be carefully designed to solve the signal integrity issue. In the current stage, the FPGA board and the ADC board are connected together via a 80-pin SCA2 cable. In the testbed design, the ADC sampling frequency is 1GHz in order to support the system bandwidth of 500MHz. The corresponding ADC output signals have maximum frequency of 500MHz. The SCA2 cable is not able to support the signals with such wide bandwidth. Because of the bandwidth limitation of the SAC2 cable, a sampling clock of 100MHz is used in the current testbed. The system bandwidth is also reduced to 50 MHz in order to keep the FPGA design valid for the case of the sampling clock of 1GHz. Once the bandwidth limitation problem is solved, the current FPGA design can be used for the system with bandwidth of 500MHz. Only minor modification

is needed. One solution is to make two adaptor boards which are attached to FPGA development board and ADC board, then connect two adaptor board though 50 Ω SMA cables. The interface solution can support signal with bandwidth up to several GHz. The adaptor board on the FPGA side is shown in Fig. 4.5.
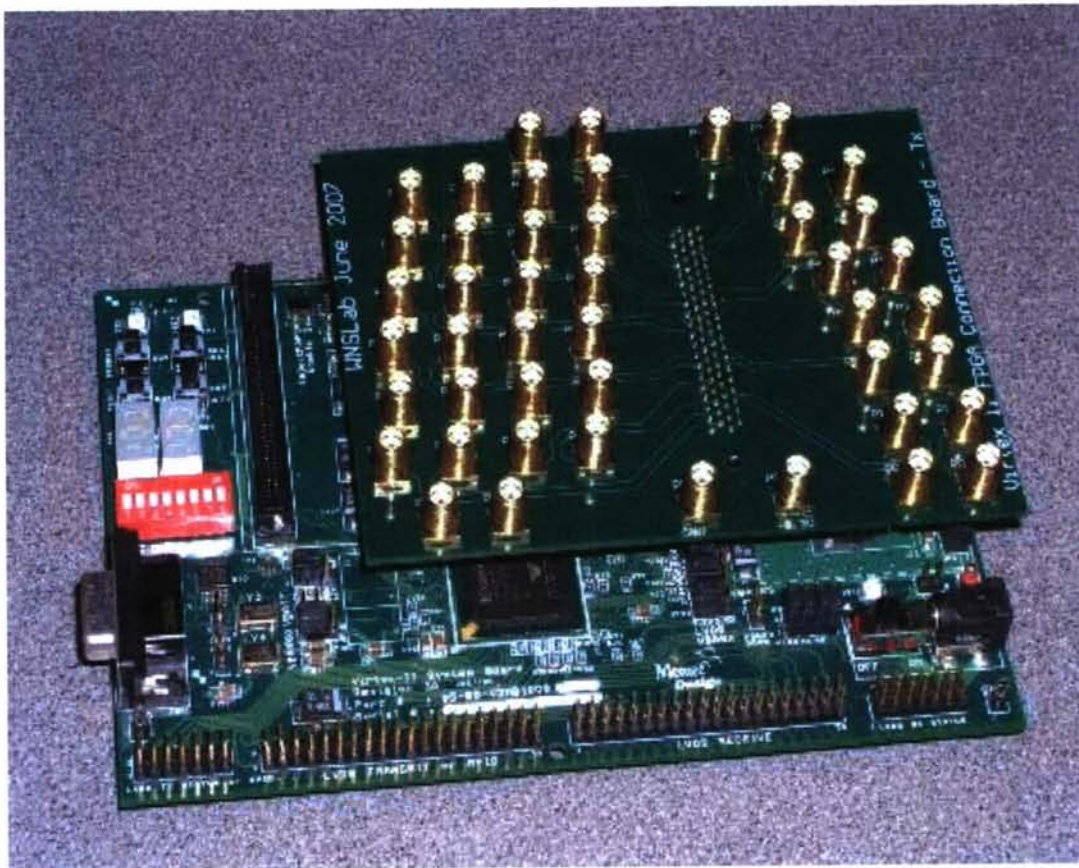

Figure 4.5: FPGA/ADC interface board.

4.4.3 Synchronization

For UWB impulse radios signal initial acquisition is extremely difficult because of the very narrow pulses with ultra low power and low duty cycle. In the testbed, timing requirement is relaxed to the symbol level. Since energy detection employed in the testbed is not able to identify signal polarity, the initial acquisition has to rely on a uni-polar sequence whose autocorrelation is typically less sharp than that of a bi-polar sequence. Optical orthogonal code (OOC) is used in the testbed for synchronization. The OOC codes can be much longer than the Barker code and exhibit better autocorrelation property, which is desirable for severe propagation cases. Two stage synchronization strategy is employed in the testbed. Tracking is not considered while the initial timing acquisition is implemented in the testbed.

Frame Structure

The frame structure shown in Fig. 4.6 consists of 208 preamble chips, 960 data symbols and 48 chips guard interval. 4 chips represent a symbol. The preamble consists of 128 chips 1, 20 chips guard and 60 chips OOC code. The OOC code is constructed by repeating a OOC of '1000100000100000000' three time and adding three 0s at the end. The preamble is used to achieve the initial timing acquisition.
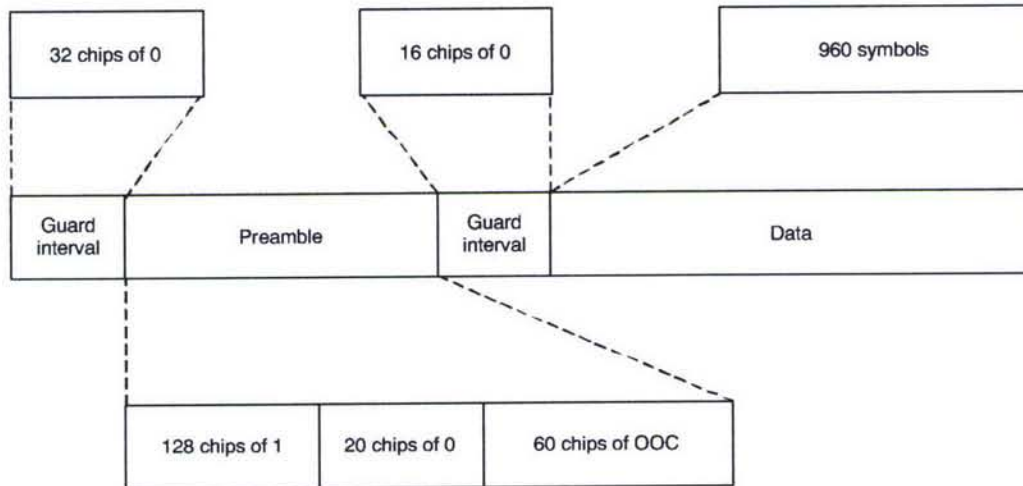

Figure 4.6: Frame stucture.

Synchronization Procedure

Firstly, the receiver is searching for the chip synchronization. The symbol and frame synchronization is based on a successful chip synchronization. In the energy detection, the correct chip synchronization point is the delay which leads a integrator to collect the maximum signal energy when the transmitter is sending the preamble. In order to achieve the initial timing acquisition quickly, a parallel searching is employed instead of a serial searching. The cost of the parallel searching is that more FPGA resources are occupied. A bank of parallel integrators followed by selection of the maximum integrator outputs is implemented in the FPGA device for the chip synchronization. The structure is shown in Fig. 4.7 where Tb is the chip duration, N is the number of integrators. The goal is to find the integrator whose output is the maximum among all integrators. The timing accuracy of the chip synchronization is related with the number of integrators N. In the testbed, 32 integrators are employed to achieve the chip synchronization. The output of the synchronized integrator is sampled at chip rate and sent to a digital correlation with 60 taps for symbol synchronization. Once the chip level synchronization is achieved, the 60 chips OOC can be used to determine the symbol synchronization and the frame synchronization in the testbed. The detection of the symbol synchronization is based on the correlation between the output of the synchronized integrator and the OOC code. The maximum output of the correlator indicates the symbol synchronization.
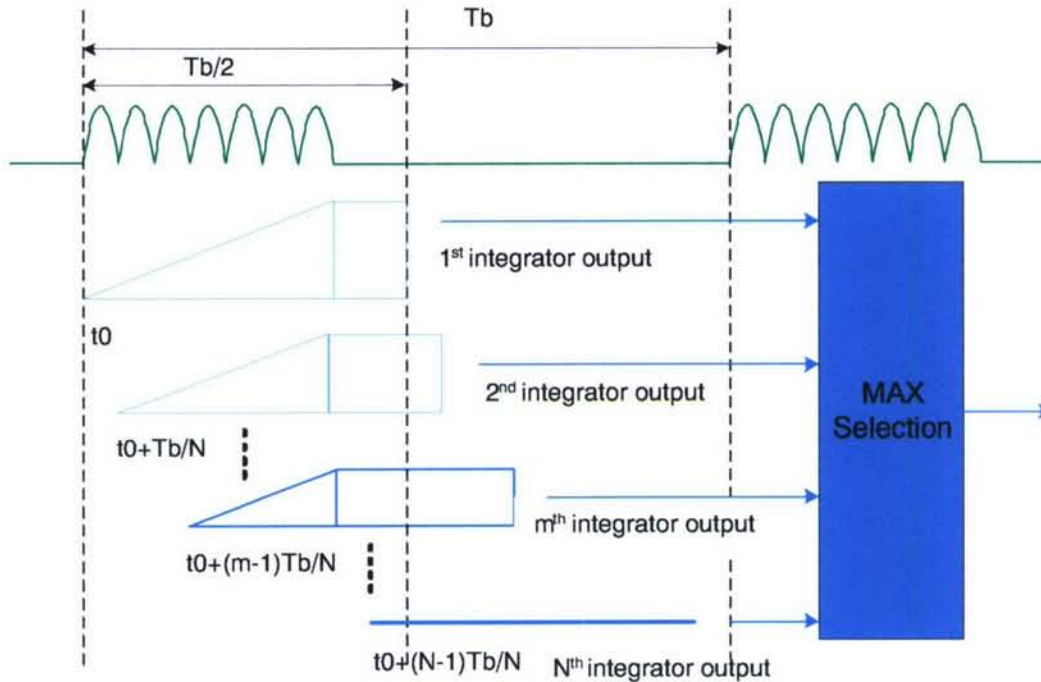
Figure 4.7: Chip level synchronization.

4.4.4 FPGA Design and Implementation

A key part of the testbed is FPGA design and implementation. All baseband processing algorithms are implemented in FPGA device. Hardware description language (HDL) is chosen as the design entry. FPGAs are designed in Verilog. Xilinx software ISE foundation with XST synthesizer is used for design synthesis and implementation. The functional and timing simulation is performed by ISE simulator. A comprehensive testbench is given to stimulate the simulation. Xilinx software Chipscope Pro enables the real time debug and verification for FPGAs. In order to achieve high performance, proper coding techniques are used in the FPGA design, like synchronous design techniques, Xilinx-specific coding and IP cores.

Transmitter Coding

The transmitter FPGA block diagram is as the same as shown in Fig. 4.2, except the empty spread spectrum block. The transmitter transmits the signal frame by frame. In each frame, the preamble is transmitted firstly, then data follows. Illustrated in the Fig. 4.8 is the flow chart for the transmitter.
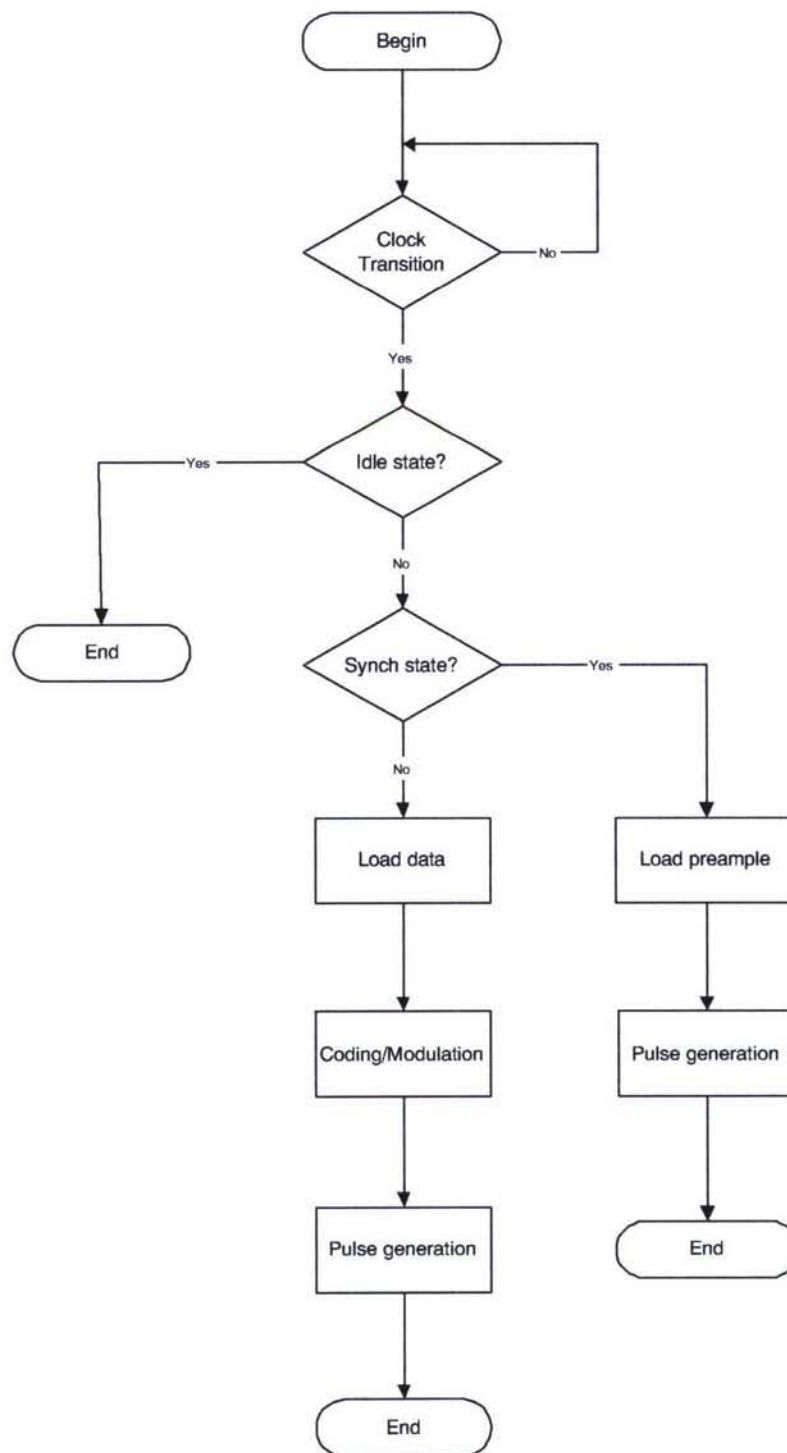
Figure 4.8: Transmitter flow chart.

The routed FPGA design in the transmitter shown in Fig. 4.9 is observed using the software Xilinx FPGA editor. The blue area indicates that the logic resources in this area are occupied by the design.
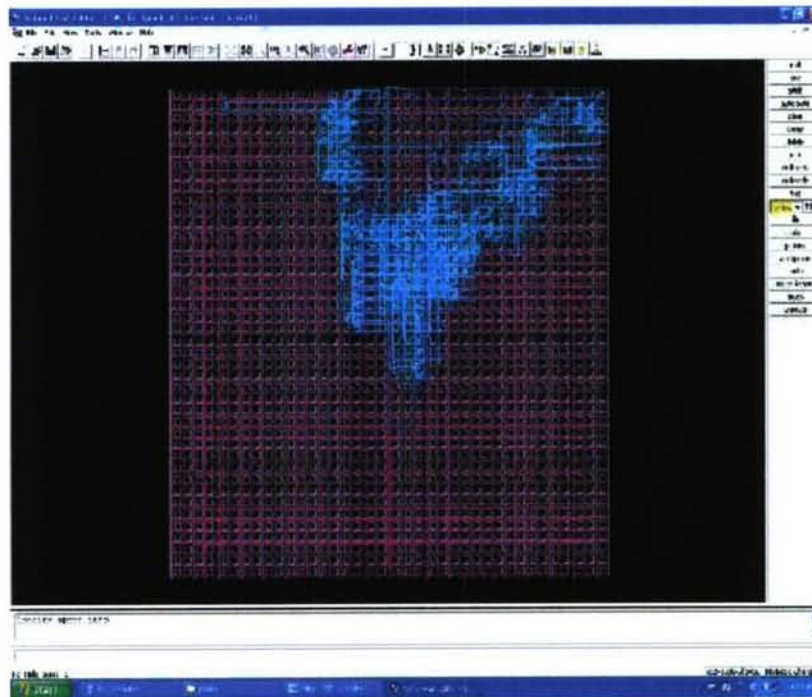
Figure 4.9: Rounted FPGA design for the transmitter.

Receiver Coding

The receiver coding is more complicate than the transmitter coding because much more digital signal processing algorithms need to be implemented in the receiver. In the receiver three states are defined. State 00: Idle state where the receiver monitors the signal arrival; State 01: synchronization state where the receiver searches for the initial timing acquisition; State 10: data transmission state where the receiver receives the transmitted data. The state transition diagram is shown in Fig. 4.10. The idle state is defined as the initial state. If the receiver detects the signal arrival in the idle state, the system enters into the synchronization state. Then if the synchronization succeeds, the system enters into the data transmission state. If the synchronization failed, the system is back to the idle state. When the data transmission is finished, the idle state takes place.

The receiver FPGA block diagram is shown in Fig. 4.3. In the testbed the de-spread spectrum block and ranging block are not implemented. Firstly, the receiver is in the idle state looking for the signal arrival. Secondly, the receiver performs the synchronization procedure. Finally, the demodulation and decoding are performed in the data transmission state. Illustrated in the Fig. 4.11 is the receiver flow chart. The flow chart for signal arrival, synchronization and signal processing are presented in Fig. [4.12 - 4.14], respectively.
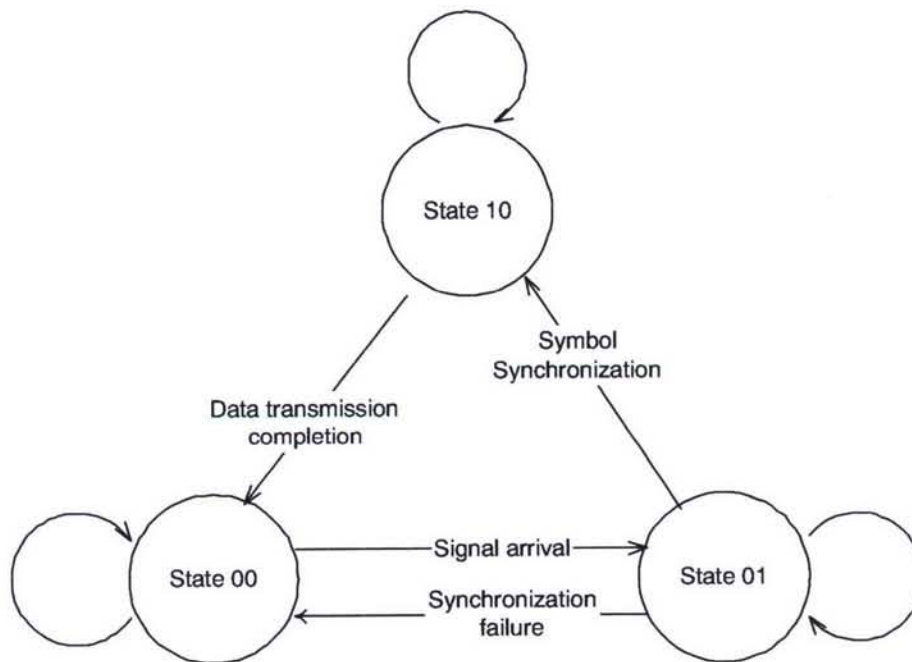
Figure 4.10: State transition diagram.

The routed FPGA design shown in Fig. 4.15 is observed using the software Xilinx FPGA editor. The blue area indicates the occupied logic resources.
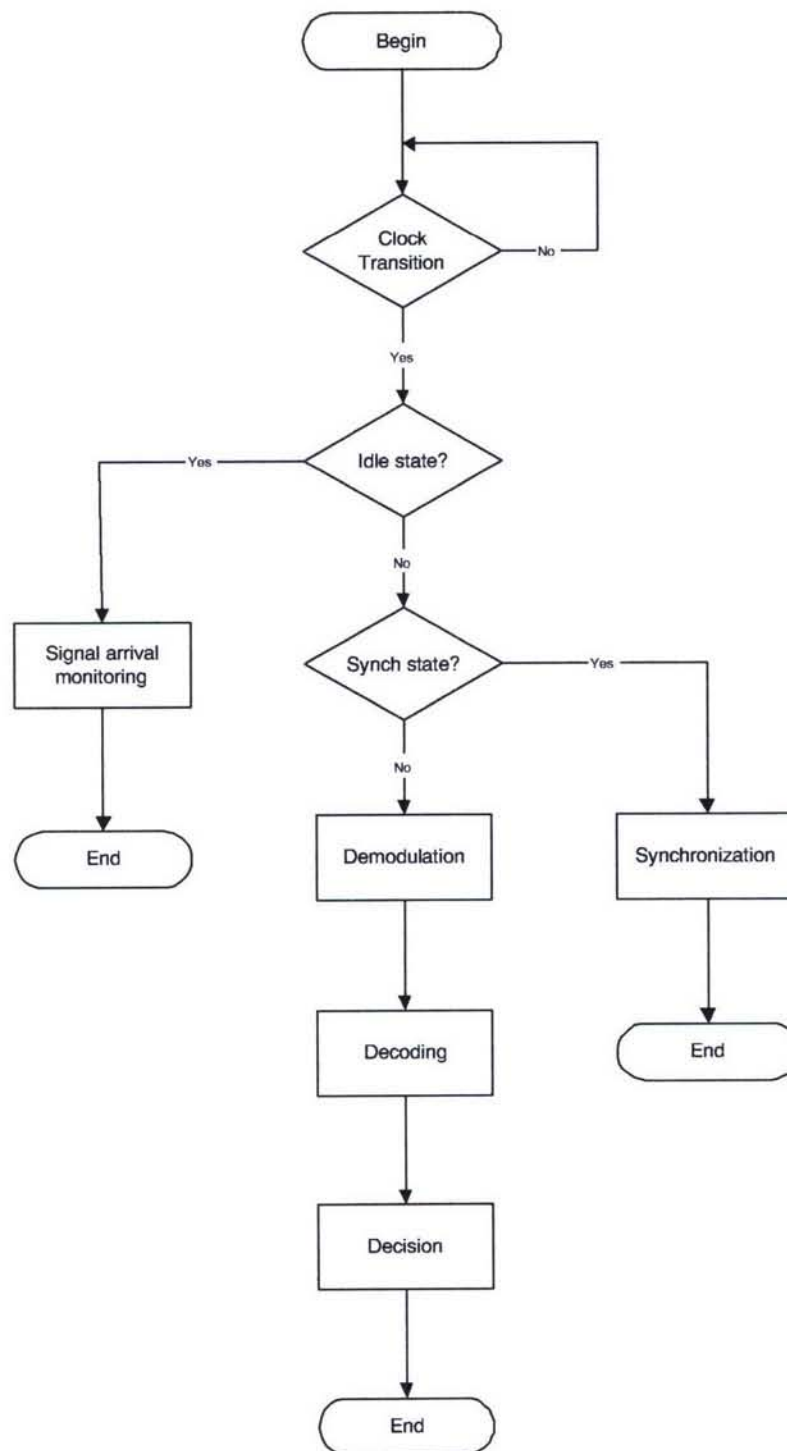
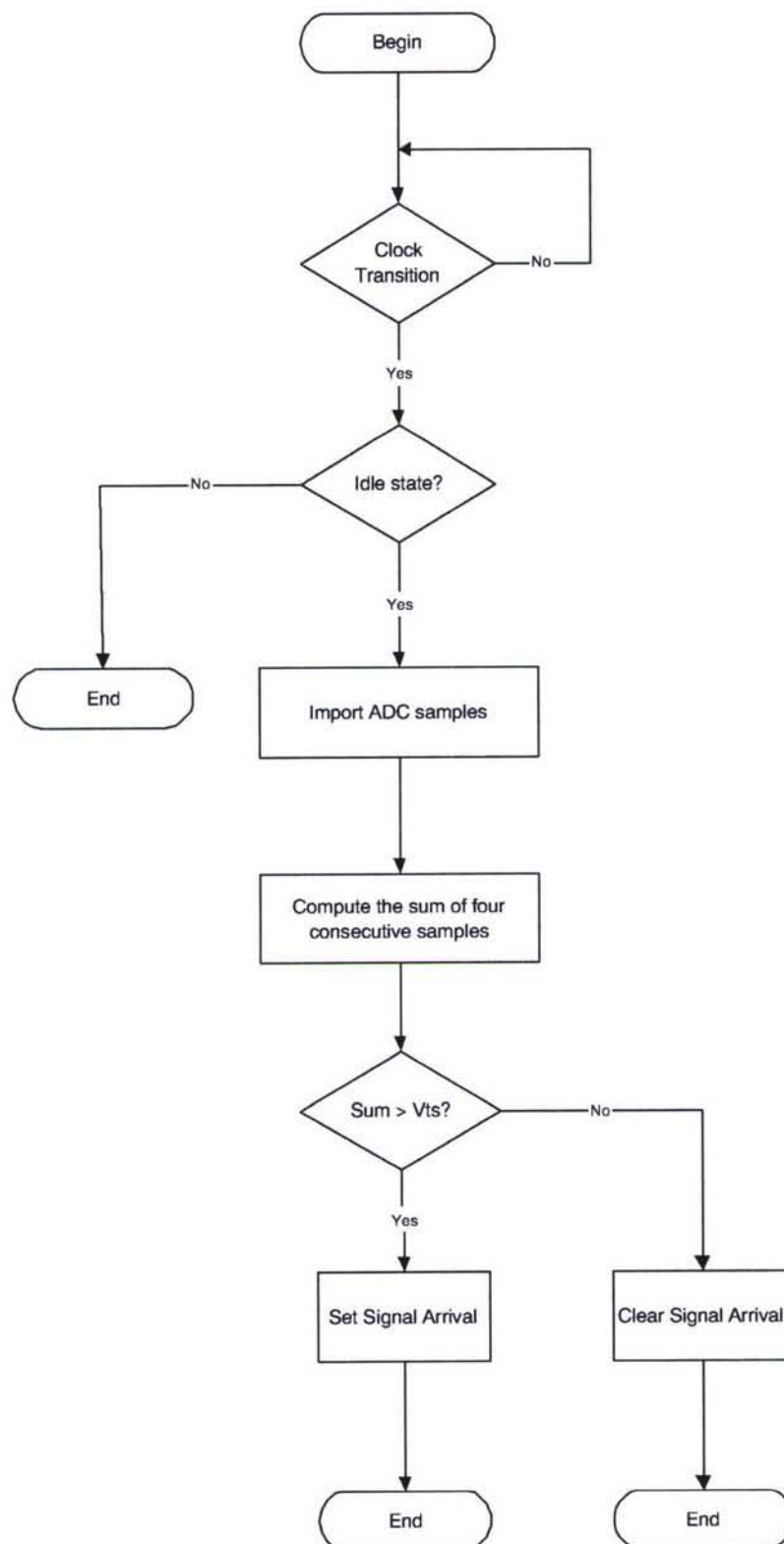Figure 4.11: Receiver flow chart.
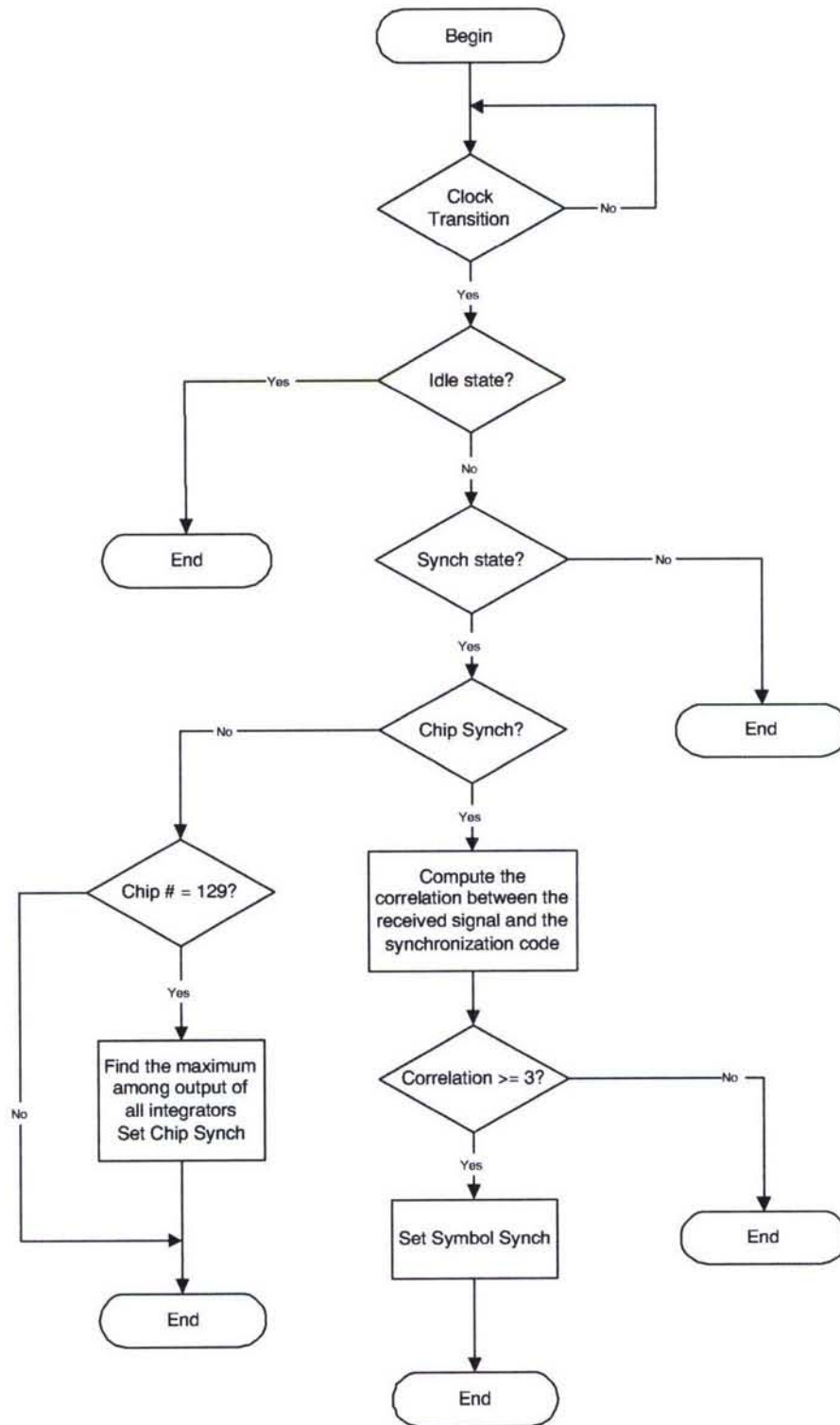
Figure 4.12: Receiver signal arrival detection.
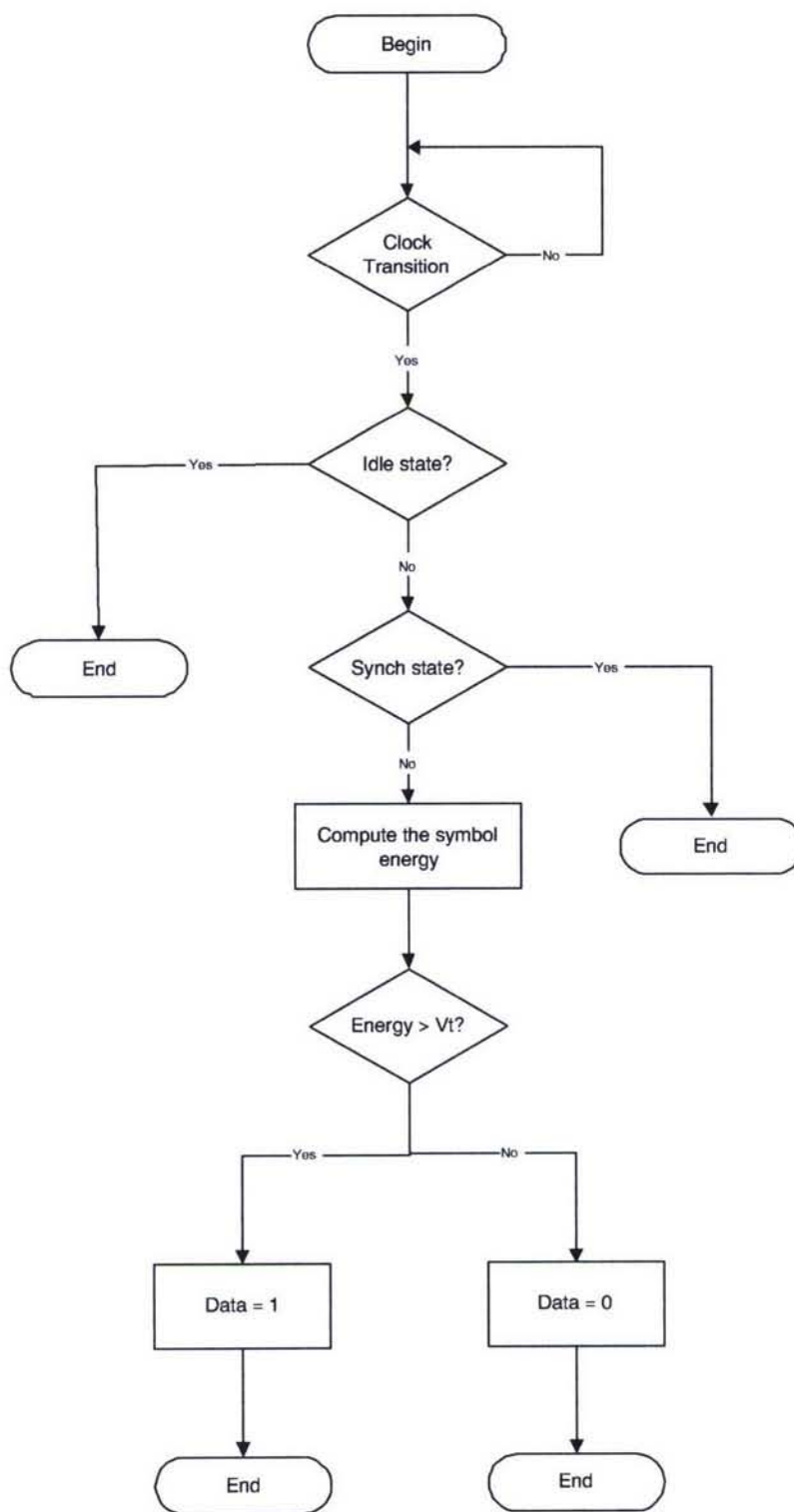
Figure 4.13: Receiver synchronization flow chart.
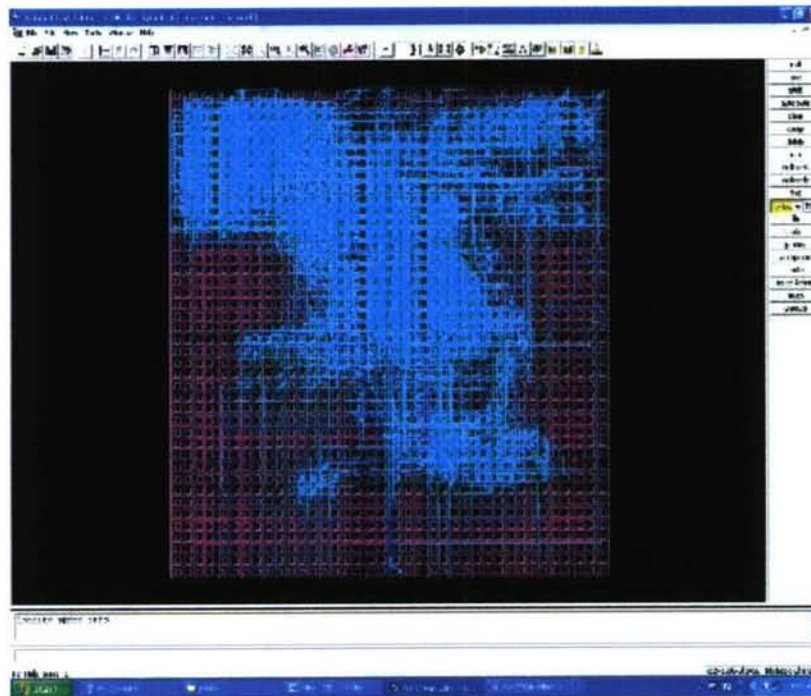
Figure 4.14: Receiver signal processing.

Figure 4.15: Rounted FPGA design for the receiver.

TABLE 4.4.4 Device utilization summary.

	Transmitter	Receiver
Number of slice flip flops	284	1533
Number of 4 input LUTs	196	2250
Number of occupied slices	306	1813
Total number of 4 input LUTs	337	2635
Number of bonded IOBs	7	52
Number of DCMs	1	2
Total equivalent gate count for the design	540657	376714

FPGA Resource Utilization

The target FPGA device is Xilinx xc2v1000-4fg456 which is one of the Virtex II platform. The detailed logic utilization for the transmitter and receiver is shown in the table 4.4.4. It can be seen that more resources are used in the receiver. The reason that the transmitter has more equivalent gate count is that a large block memory is used to store the transmitting data.

4.4.5 System Debug and Verification

The testbed illustrated in Fig. 4.16 is a complete end to end UWB system with over air synchronization. The system has been developed and tested in Wireless Networking System Laboratory at Tennessee Technological University. The transmitter is placed on the gray desk. The receiver is on the desk with a purple cover. The distance between

the transmitter and the receiver is 4 meters.

Figure 4.16: UWB testbed.

The transmitter and receiver are also shown in Fig. 4.17 for details.

Listed below are instruments used for system debugging and verification:

- Tektronics Communication Signal Analyzer CSA8000B

- Tektronics Sampling module 80E03

- Tektronics Passive Probe P6109

- Tektronics Digital Phosphor Oscilloscope TDS7104

- Tektronics Logic Analyzer TLA611

- Agilent Logic Analyzer 16803A

- Agilent Function Generator 33220A

- Rohde Schwarz Signal Generator SMIQ03B

- Rohde Schwarz Spectrum Analyzer FSEM20

Measurement Results for the Transmitter

The time domain waveform shown in Fig. 4.18 is measured at the transmitter output using Communication Signal Analyzer CSA8000B with the sampling module 80E03. The test point is the SMA connector. The amplitude of the signal is 450mV. The width of pulse is 5ns. The pulse repetition frequency is 6.25MHz.
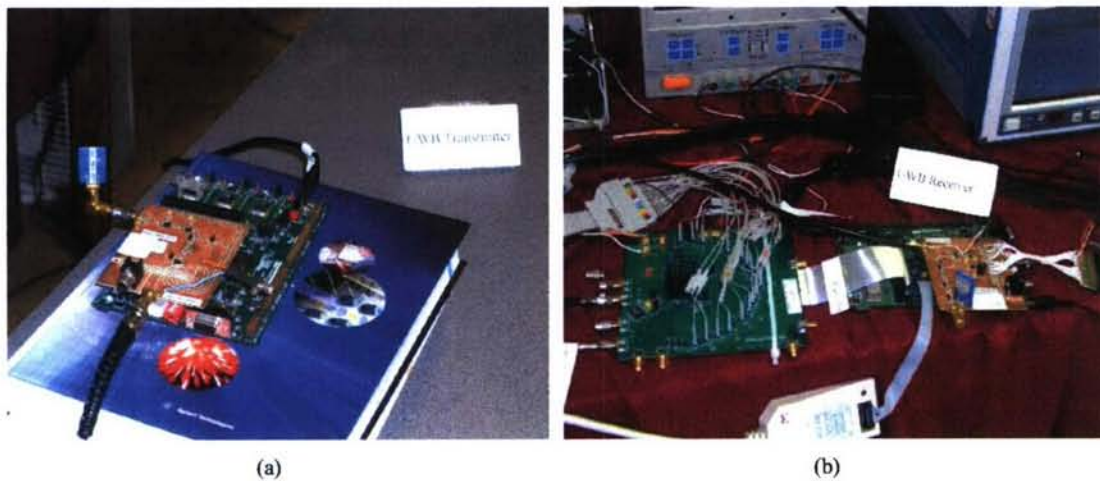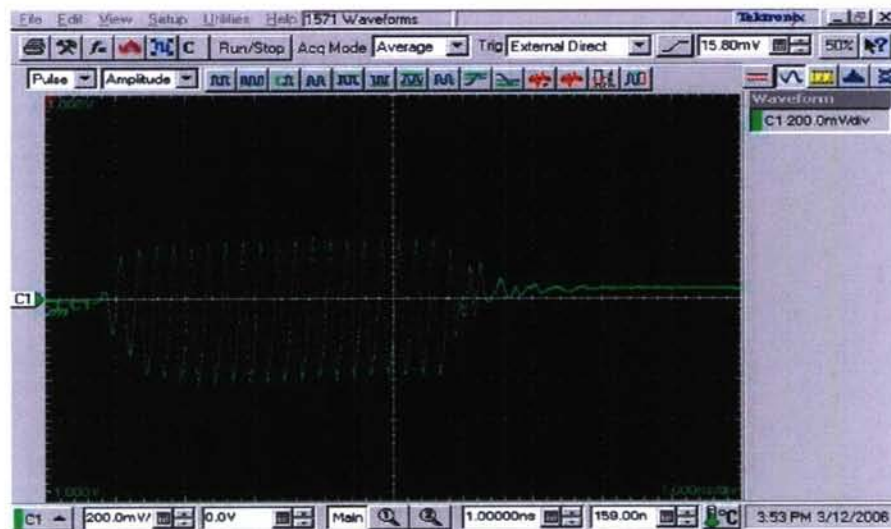
Figure 4.17: (a) Transmitter. (b) Receiver.

Figure 4.18: Transmitter output waveform.

The signal spectrum shown in Fig. 4.19 is measured by using the Spectrum Analyzer FSEM20. The center frequency is 4.02GHz. Bandwidth is 400MHz. The power level is -27.16dBm.

Measurement Results for the Receiver

When the system is running, some output signals of the receiver shown in Fig. 4.20 can be observed by using Digital Phosphor Oscilloscope TDS7104. The yellow waveform is the analog signal measured at the output of the square law detector. The green signal is the square waveform used to trigger the digital oscilloscope. The blue signal in the middle is the output data of the receiver. It is a digital signal generated by the FPGA device. The received data pattern shown on the screen is 1010110011110000 which agrees with the transmitted data. It concludes that the end
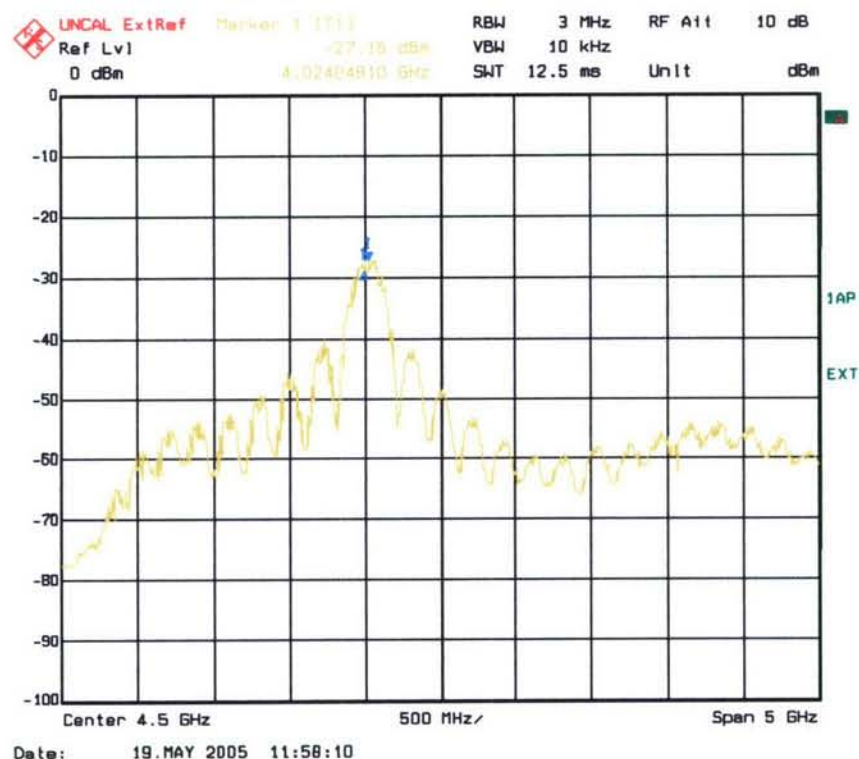
Figure 4.19: Transmitted signal spectrum.

to end UWB system is working properly in the office environment.

4.4.6   Future Work

In the current stage we are working on the high speed FPGA/ADC interface. A system performance evaluation platform is also being built. Once the work is done, more system performance tests will be performed in different environments, especially for RF harsh environments. The testbed platform can be evolved to more advanced UWB communication systems, such as chirp time-reversal UWB system.

Figure 4.20: Receiver waveforms.

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